

Compal confidential

Schematics Document

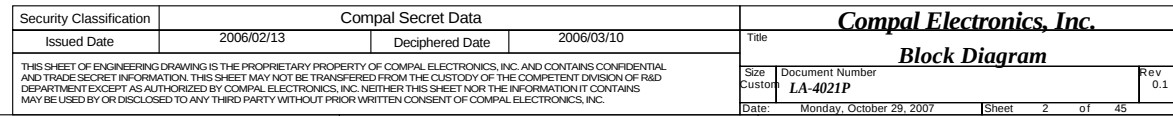
Mobile Penryn uFCPGA with Intel Cantiga_GM+ICH9-M SFF core logic

SKYY

2007-10-26



Security Classification		Compal Secret Data		Title	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Cover Sheet	
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Voltage Rails (0 MEANS ON X MEANS OFF)

power plane State	+B	+5VALW +3VALW +3VM +1.05VM	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +0.9V
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build
CONN@ : means ME part.
45@ : means install after SMT.

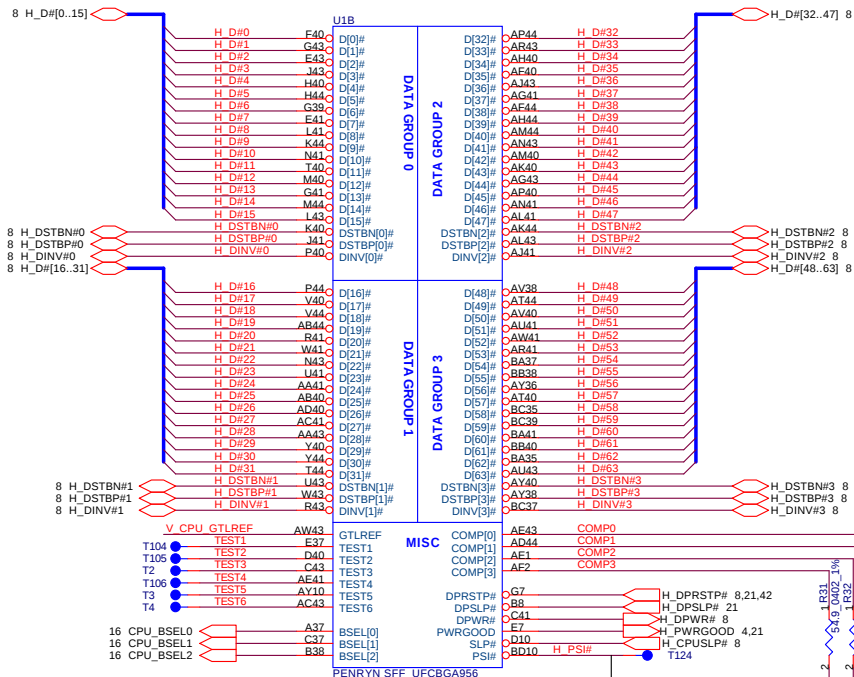
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

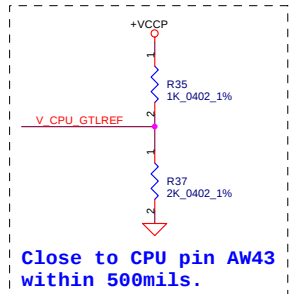
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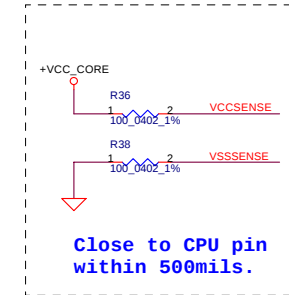
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

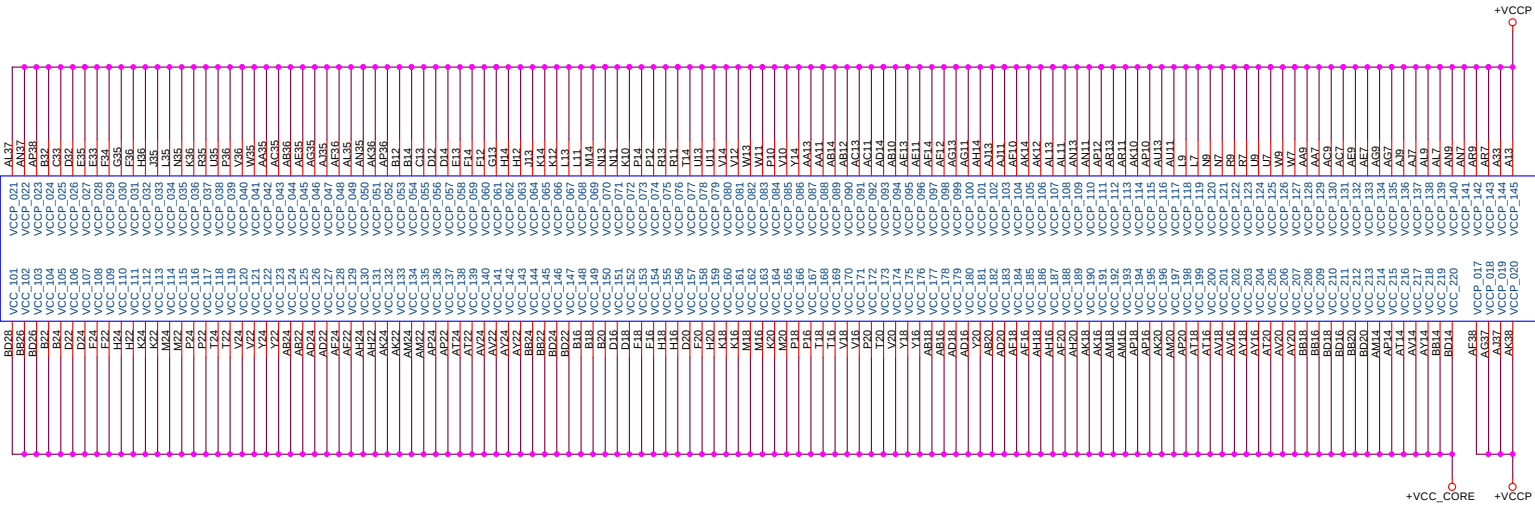
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



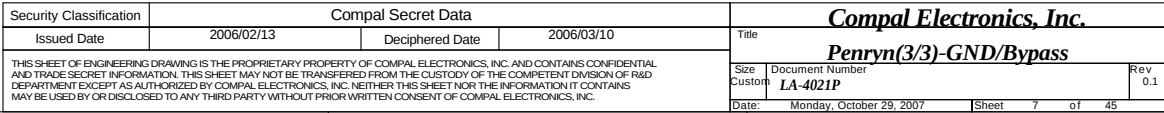
Length match within 25 mils. The trace width/space/other is 20/7/25.

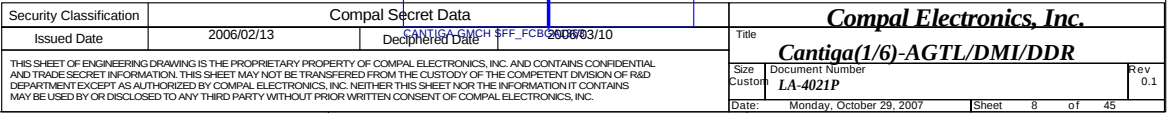




U1F
PENRYN SFF_UFCBGA956

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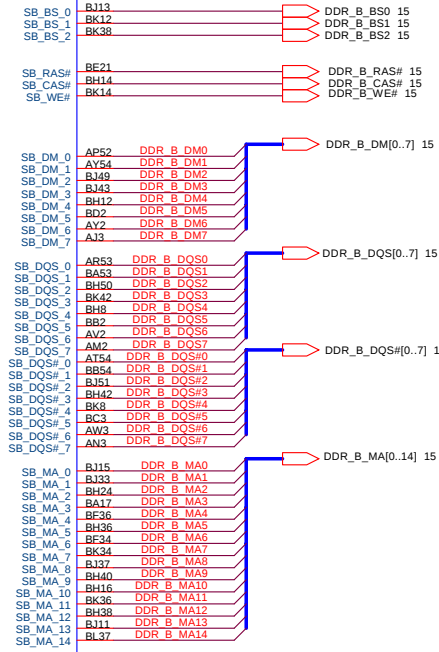
CANTIGA GMCH SFF_FCBGA1363

DDR SYSTEM MEMORY A



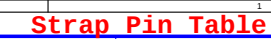
CANTIGA GMCH SFF_FCBGA1363

DDR SYSTEM MEMORY B

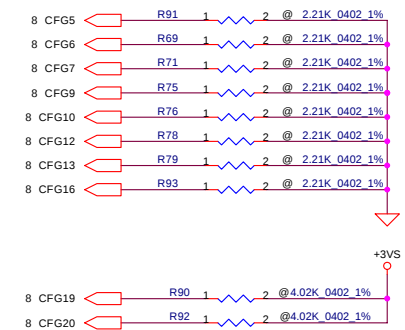


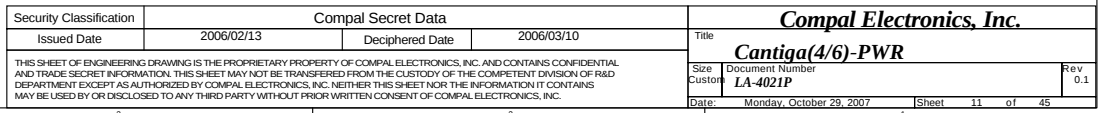
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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Cantiga(2/6)-DDR2 A/B CH	
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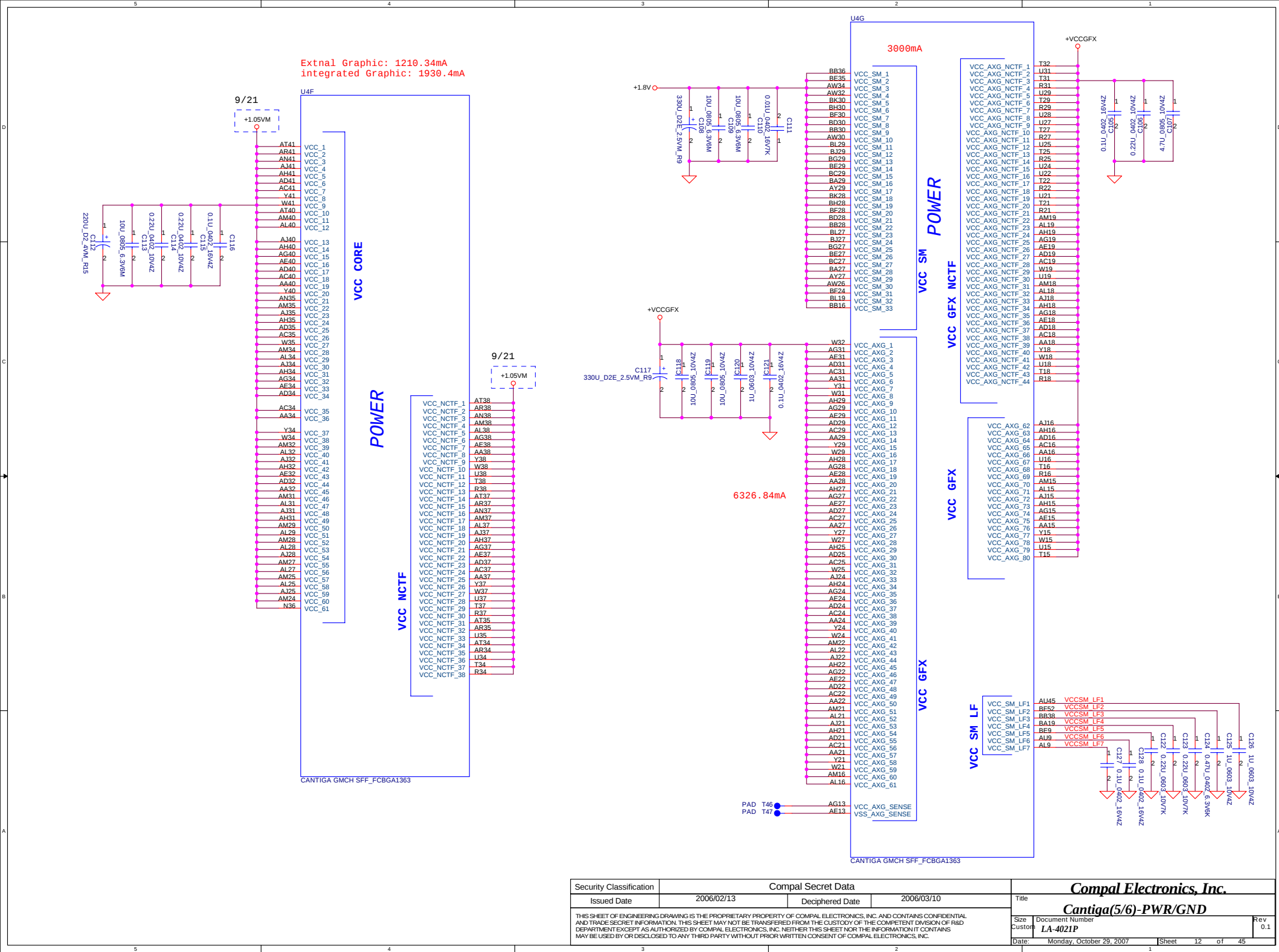
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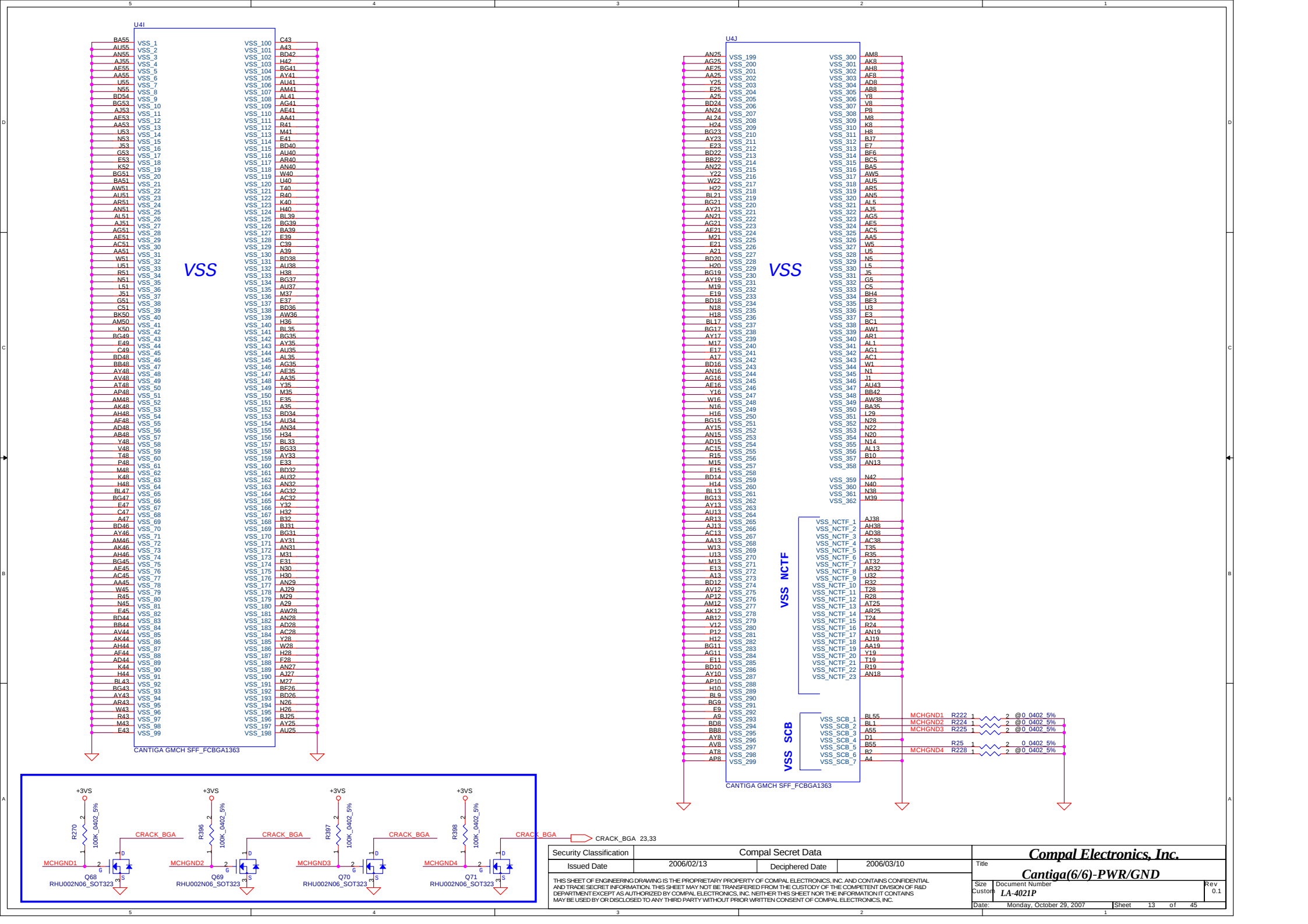
Setup Pin Table	
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

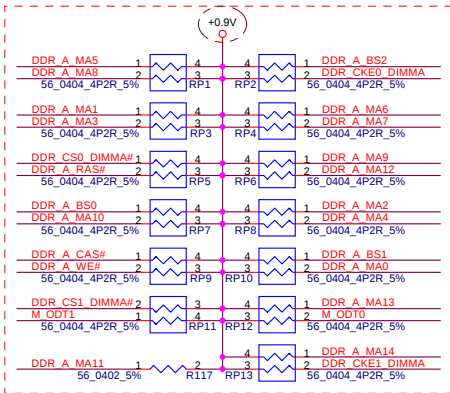
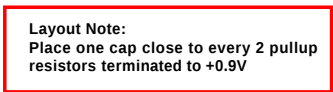
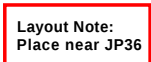




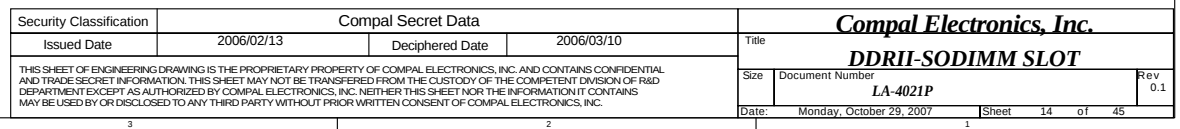


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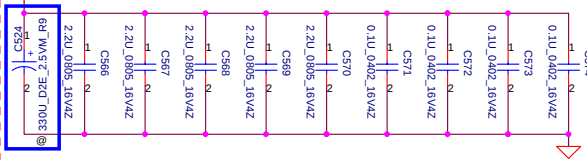
Layout Note:
Place these resistor
closely JP9,all
trace length Max=1.5"



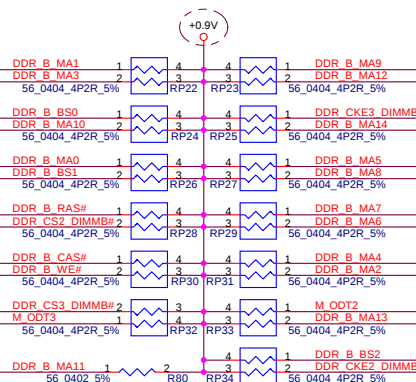
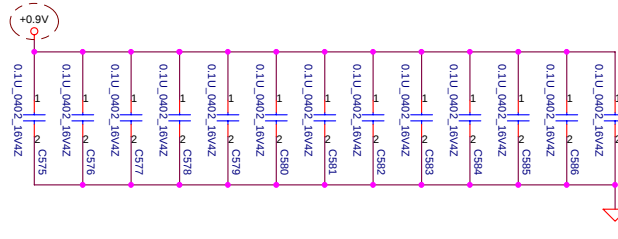
9 DDR_B_DQS#[0..7] 
 9 DDR_B_D[0..63] 
 9 DDR_B_DM[0..7] 
 9 DDR_B_DQS[0..7] 
 9 DDR_B_MA[0..14] 

Layout Note:
Place near JP34

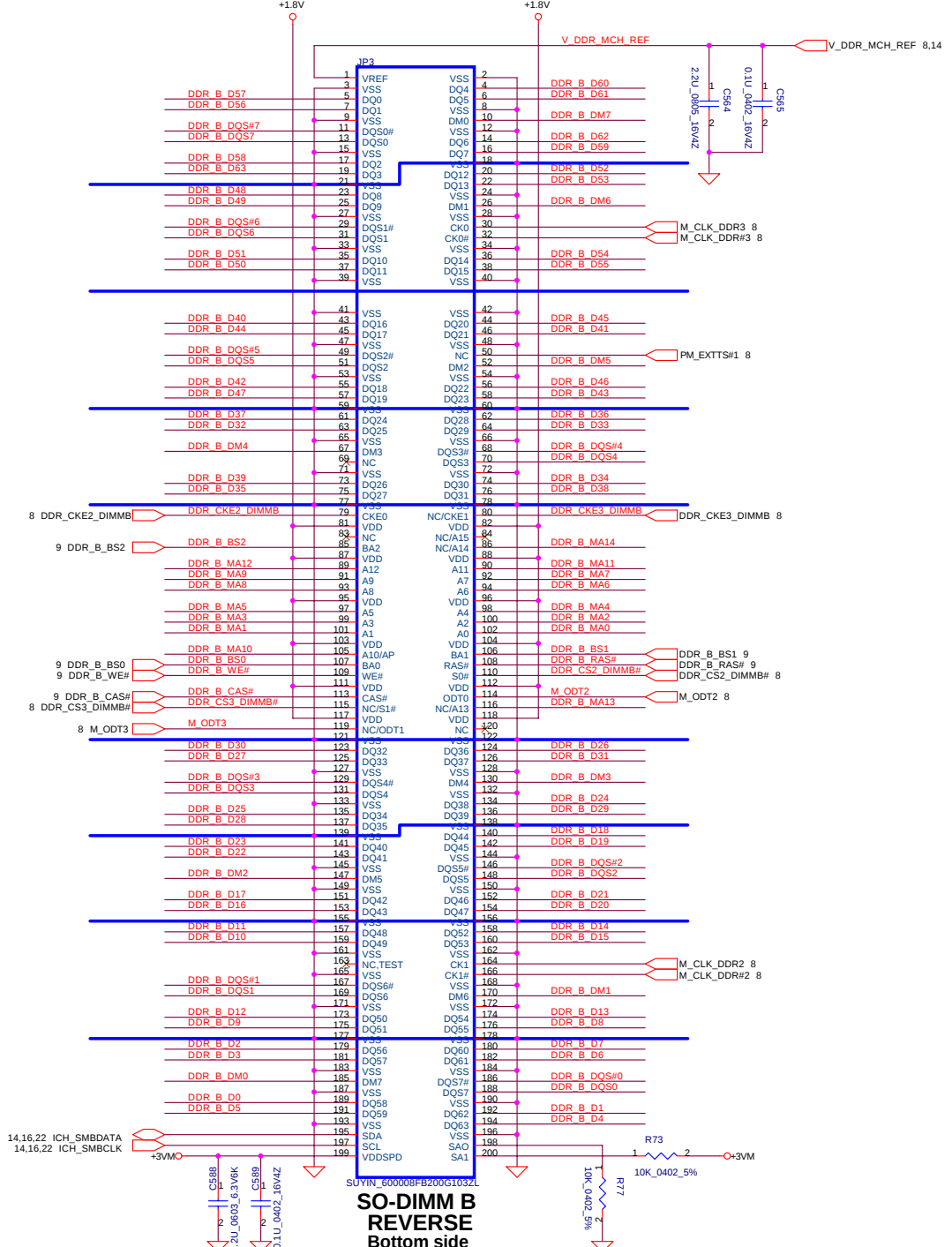
+1.8V Reserve C524. 9/26



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

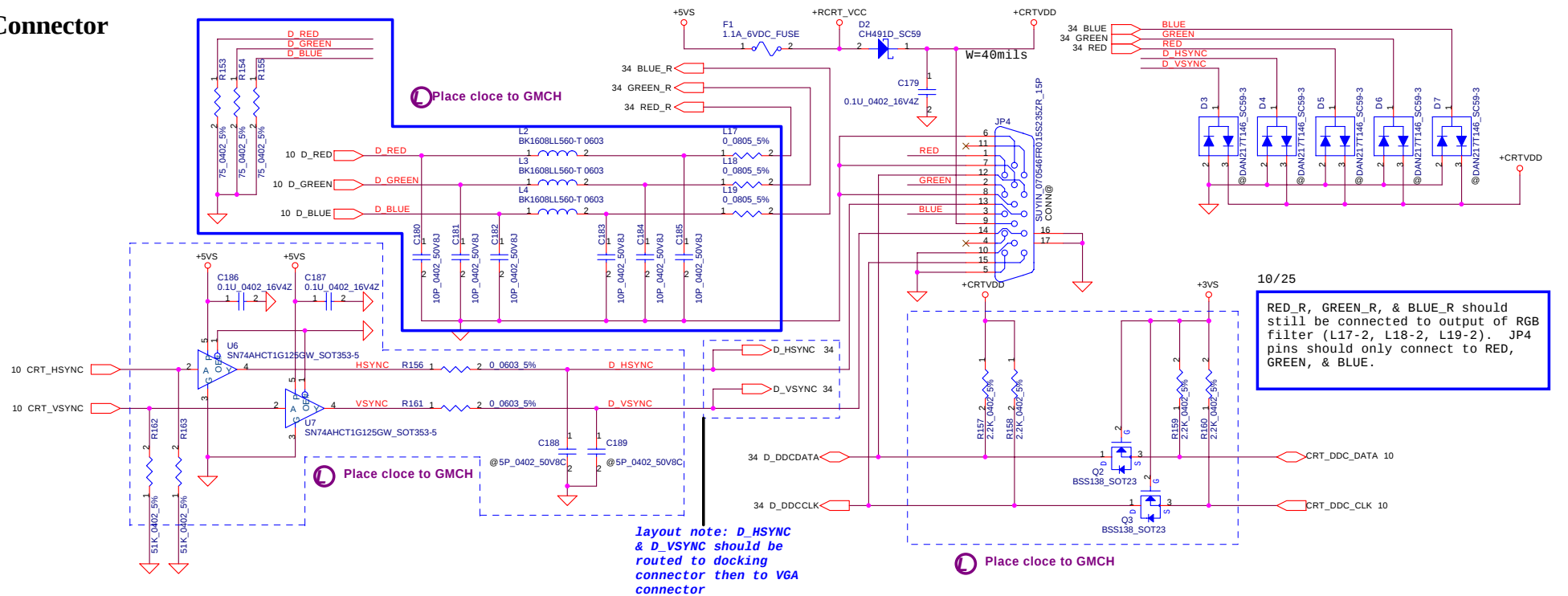


Layout Note:
Place these resistor closely JP10, all trace length Max=1.5"



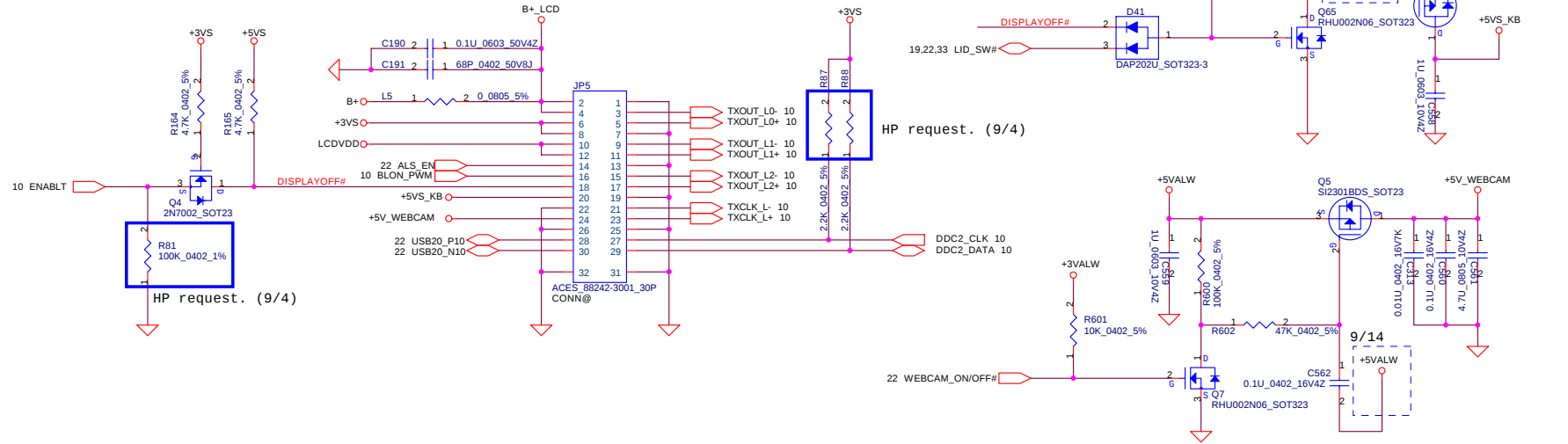
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CRT Connector

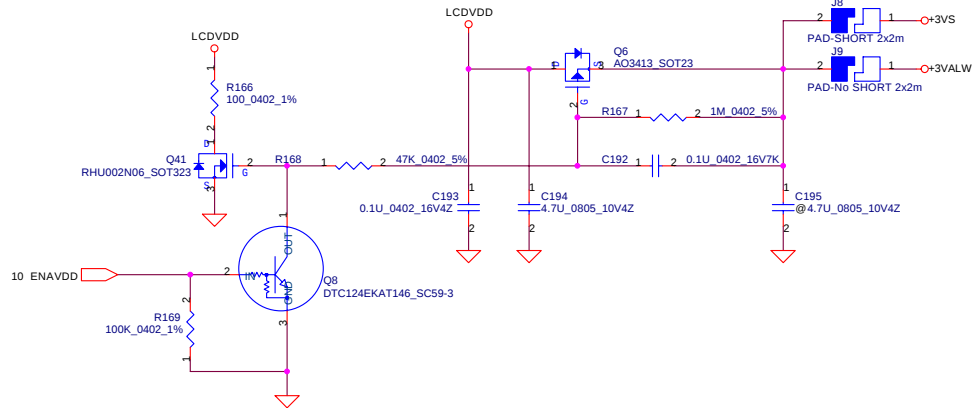


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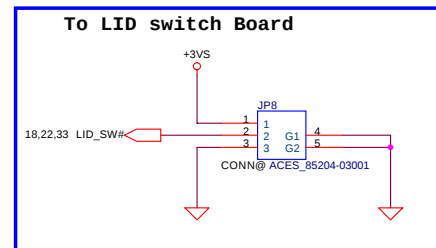
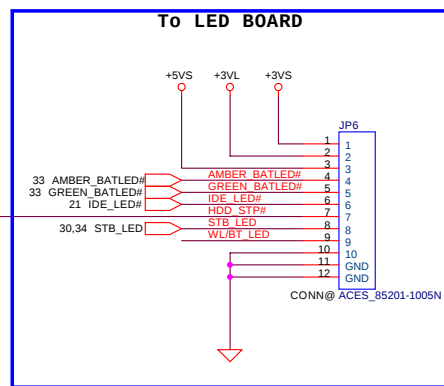
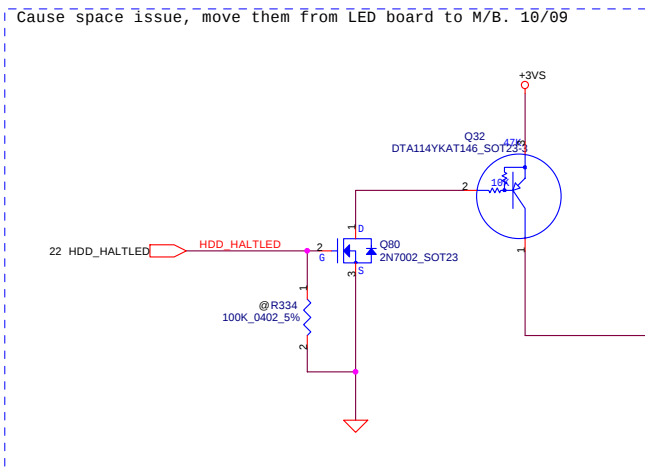
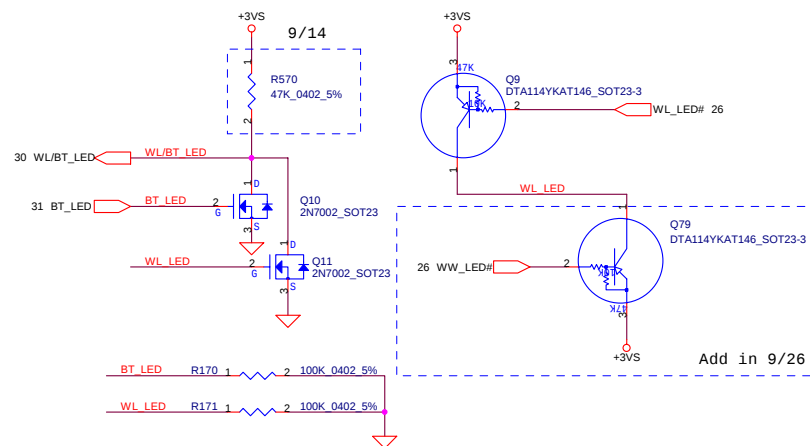
LCD/PANEL BD. CONN.



LCD POWER CIRCUIT

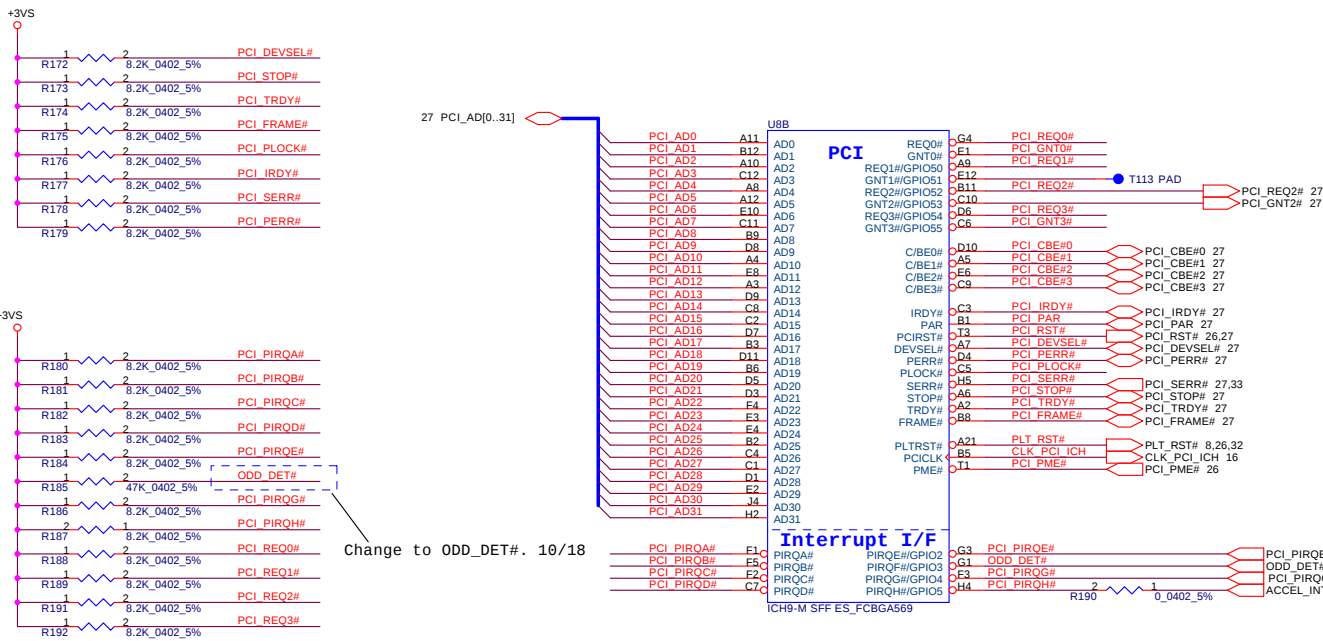


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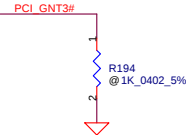


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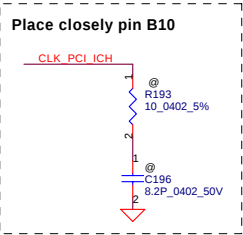
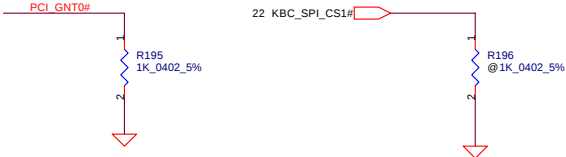
Compal Electronics, Inc.



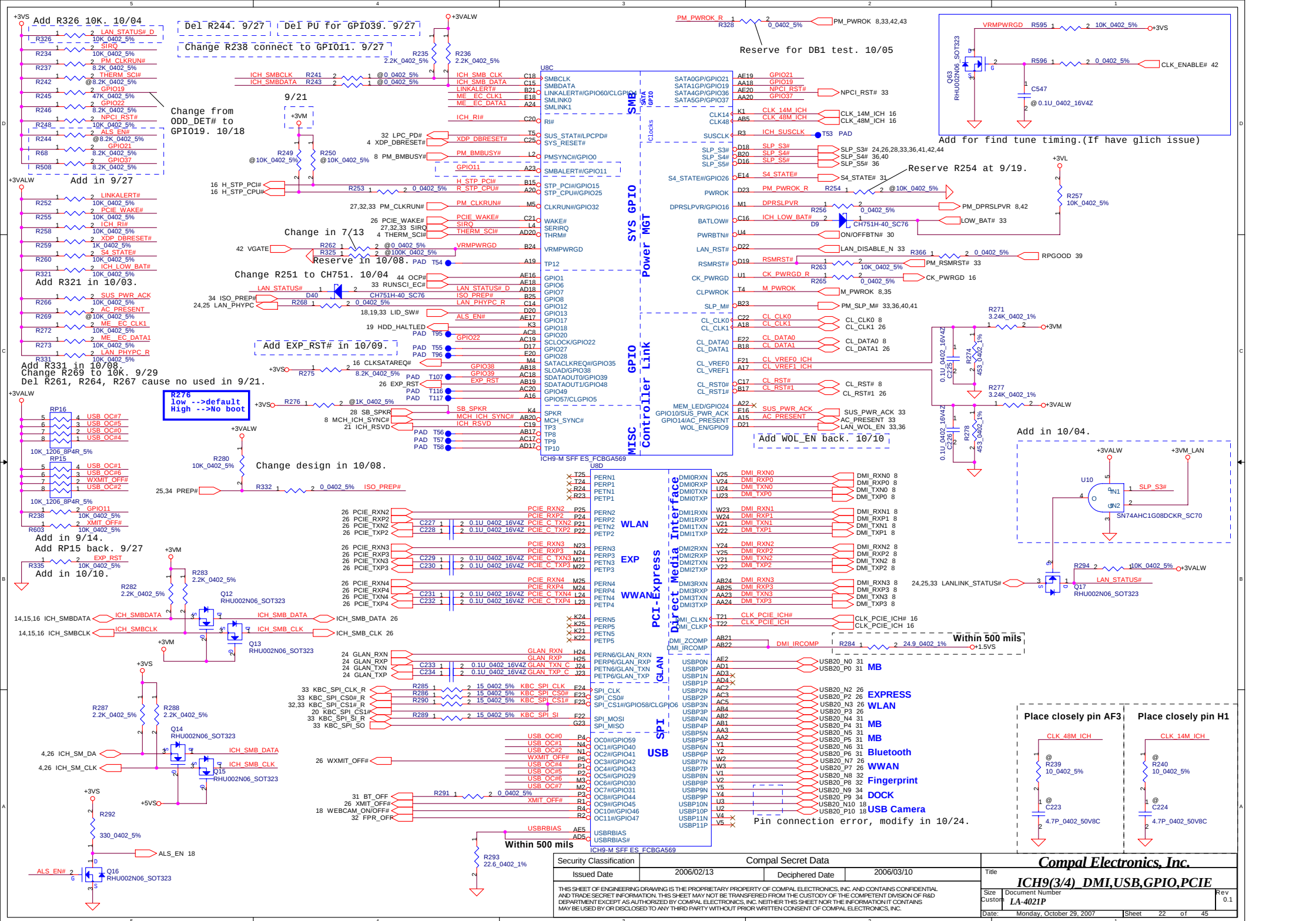
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *

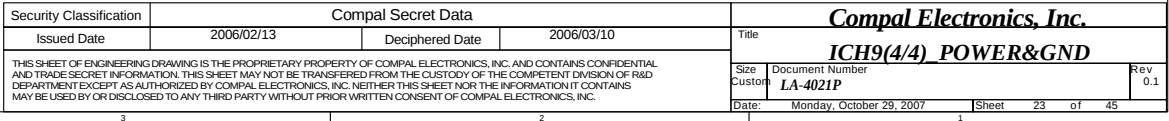


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC

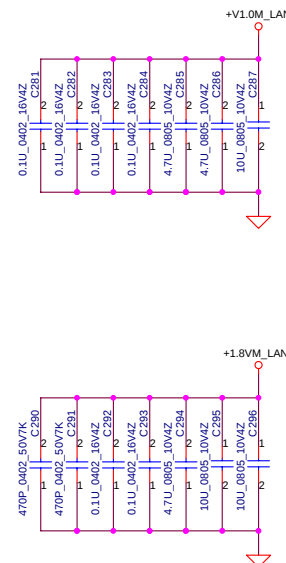
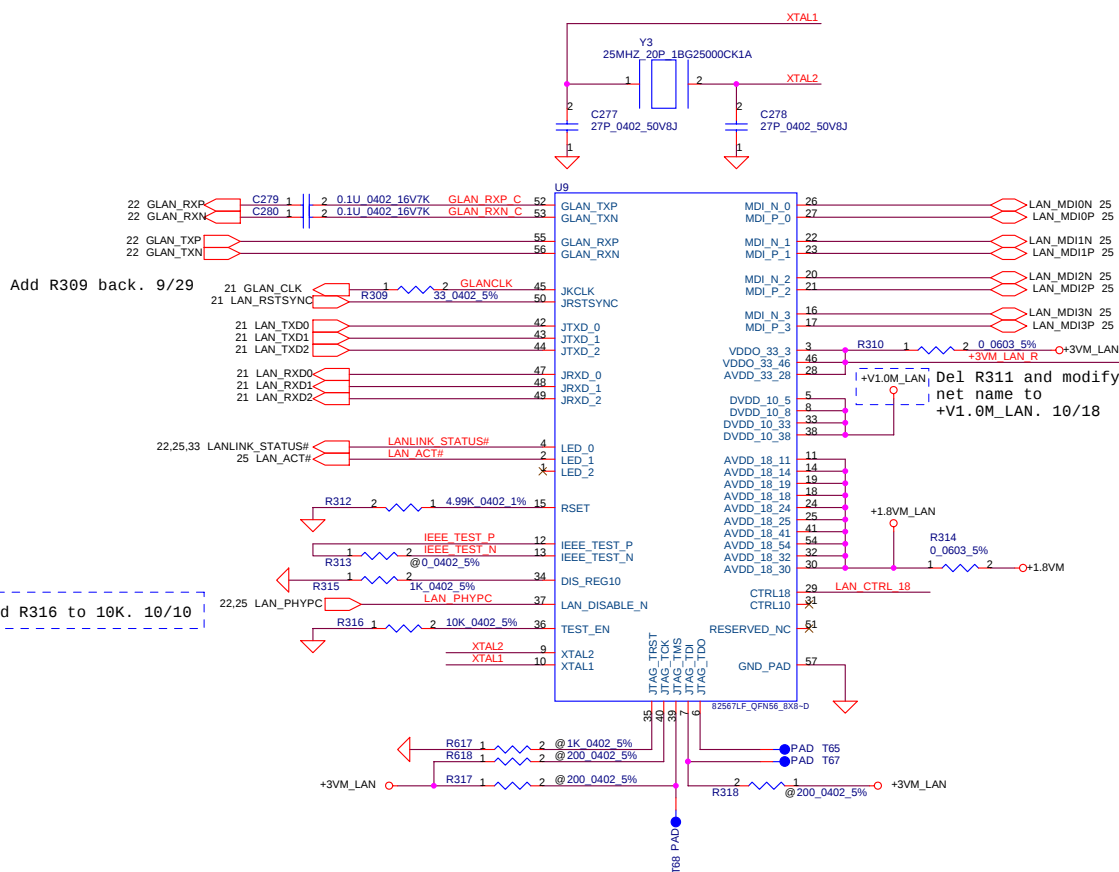
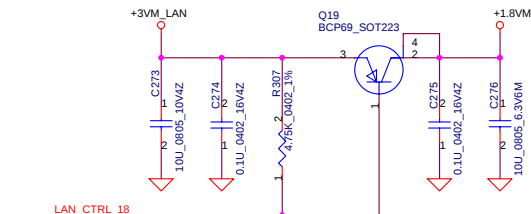
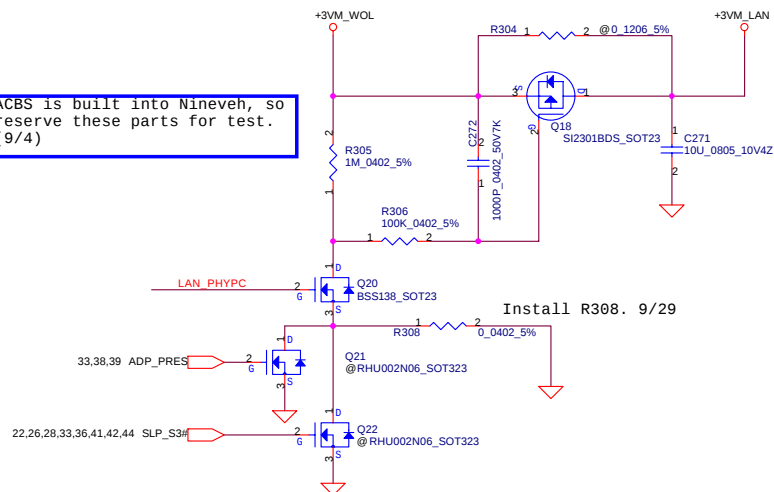


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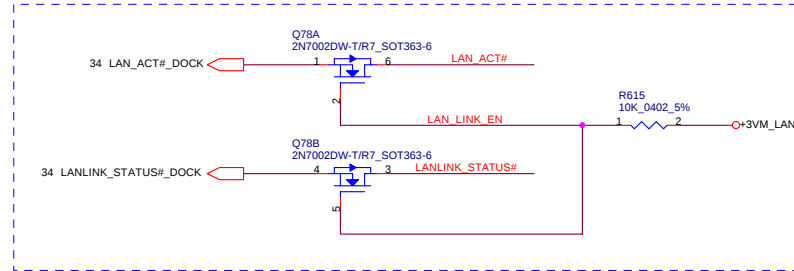
ACBS is built into Nineveh, so reserve these parts for test.
(9/4)



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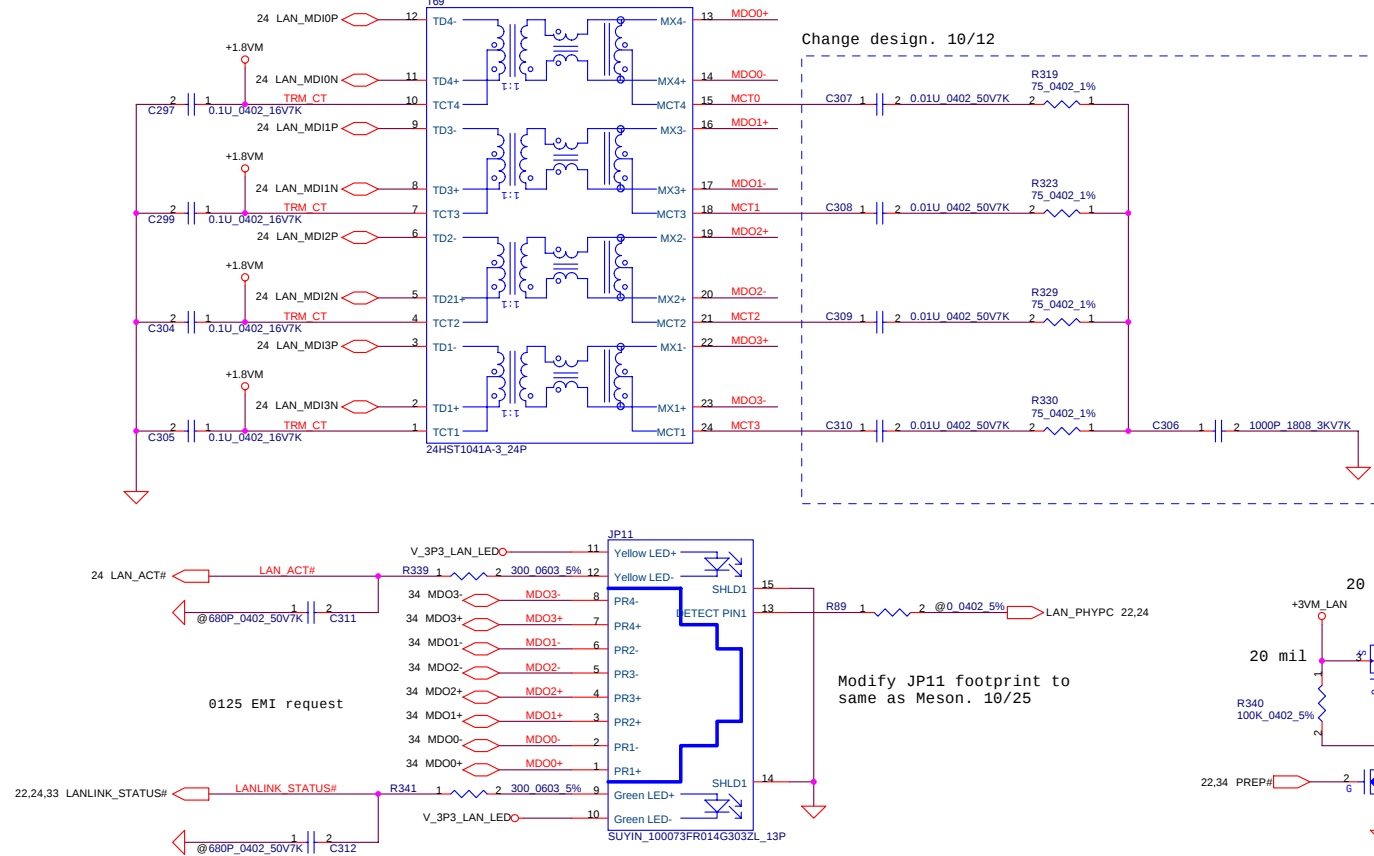
Del LAN ENERGY DET cause already inside the B0AZ. 9/27

LAN status/link level shift. 9/21



Delete all termination cause they are already inside B0AZMAN. 9/28

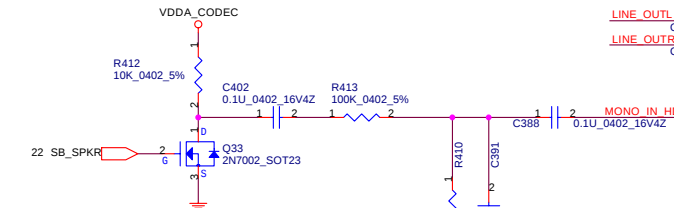
Pin Swap. 10/05
Swap P & N. 10/09



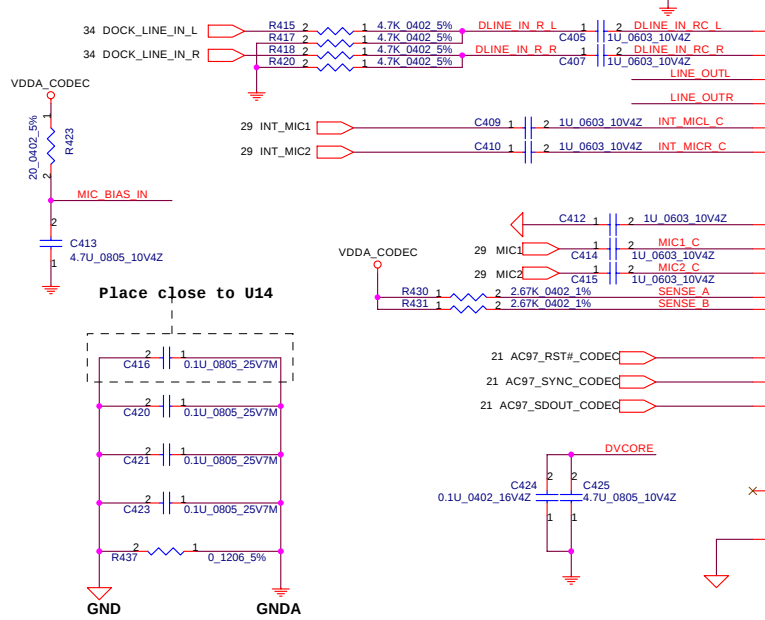
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AMP. FOR INTERNAL SPEAKER

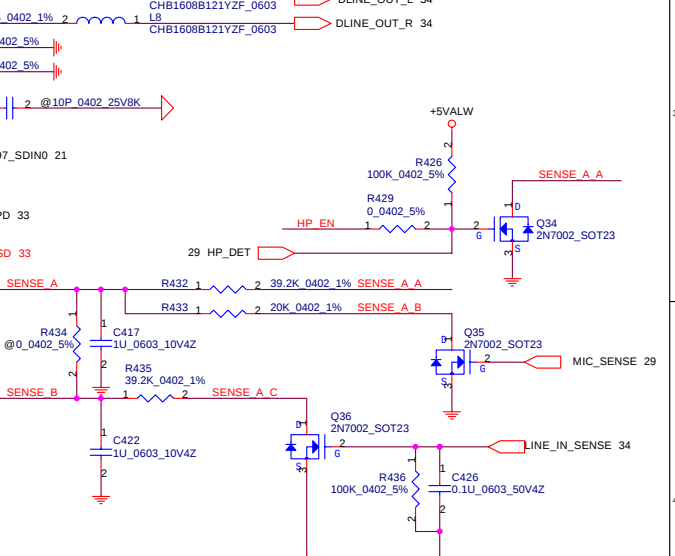
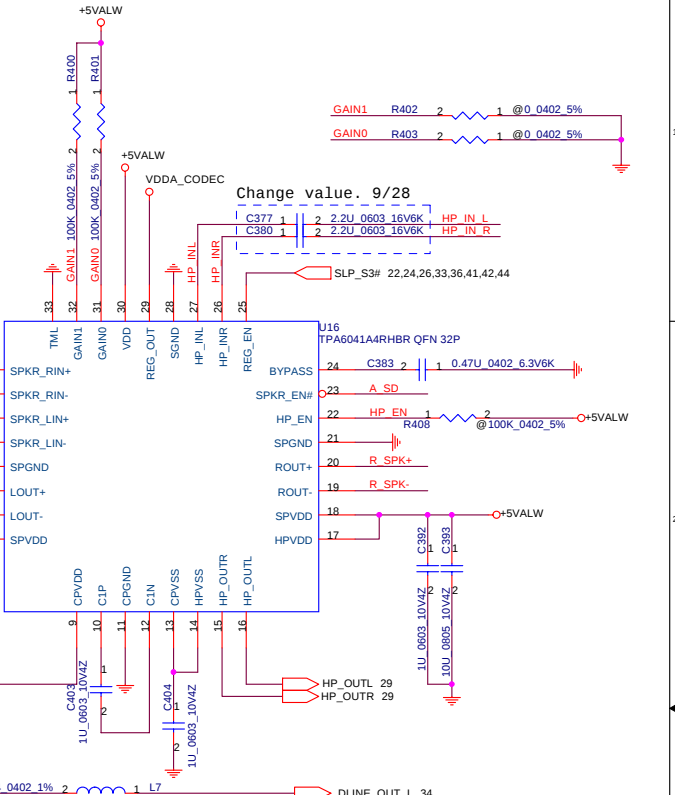
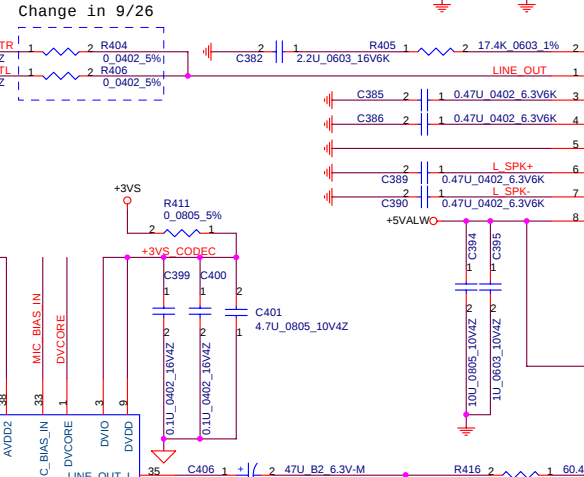
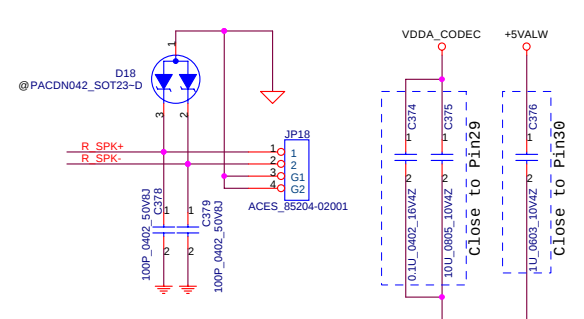
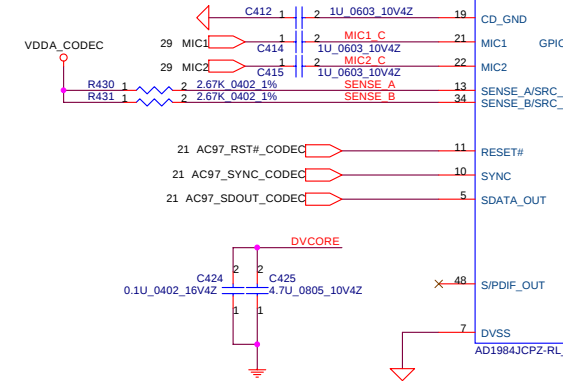
TPA6044 no longer needed. So delete BOM options & co-layout components for TPA6044. SGND and SGND1 nets can also be deleted. Only TPA6041 will be supported. 9/5



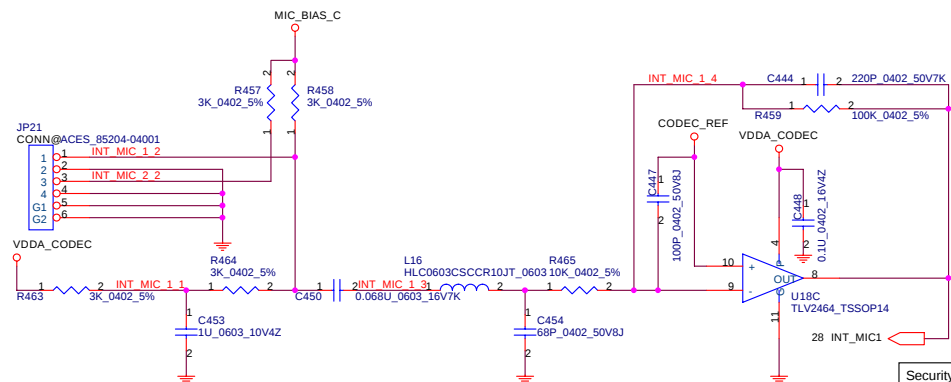
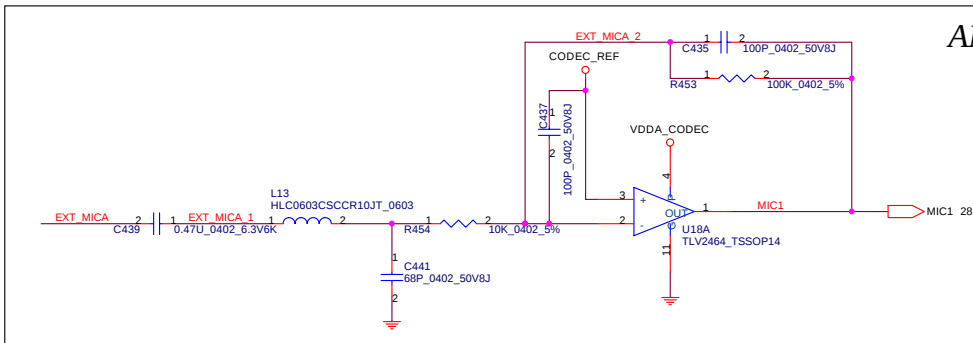
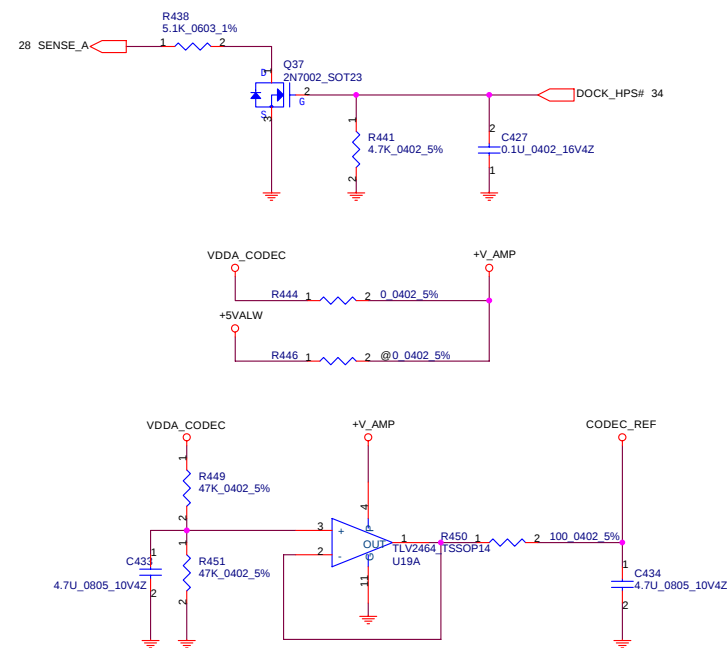
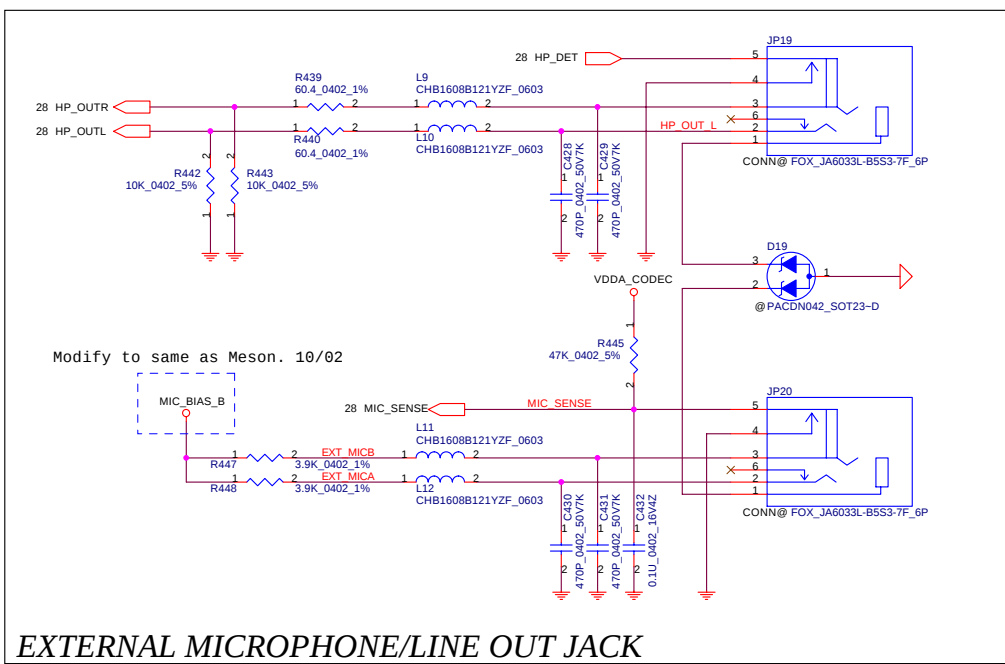
Delete PCM_SPK, Q32, R407, C387, R409. Leave circuitry to support SB_SPKR. 10/8



Place close to U14

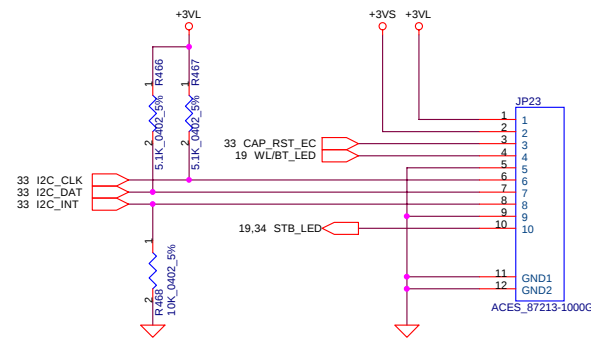


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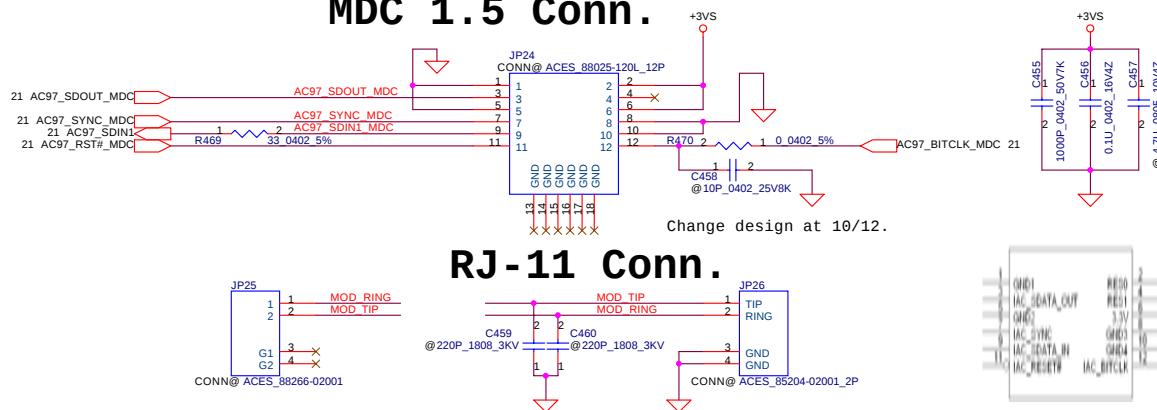


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					Size	Document Number	Rev
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SWITCH BOARD.

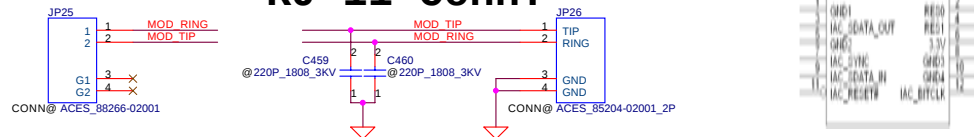


MDC 1.5 Conn.

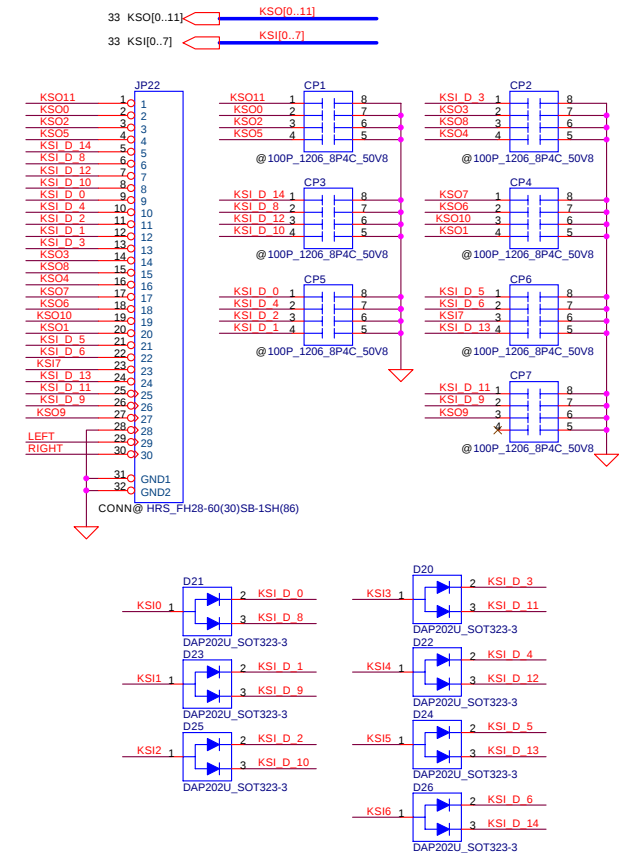


Change design at 10/12.

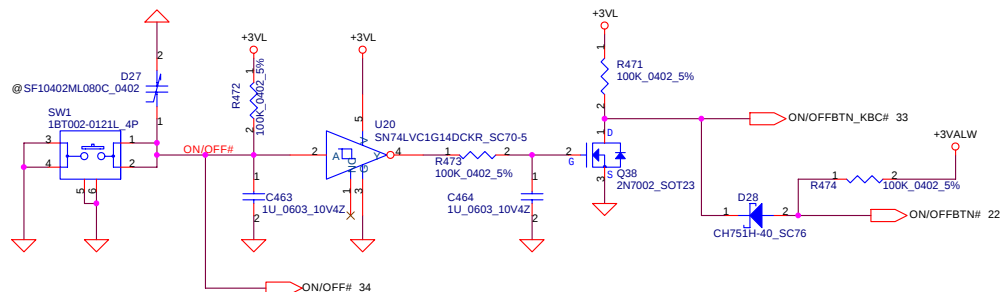
RJ-11 Conn.



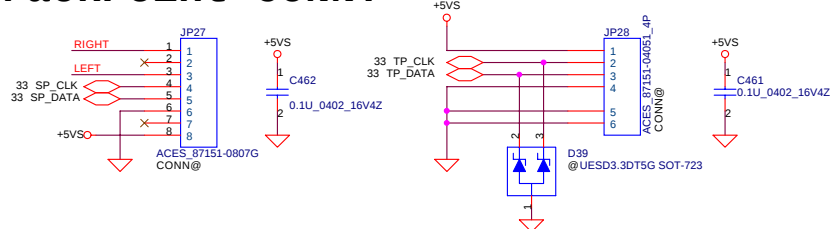
INT_KBD CONN.



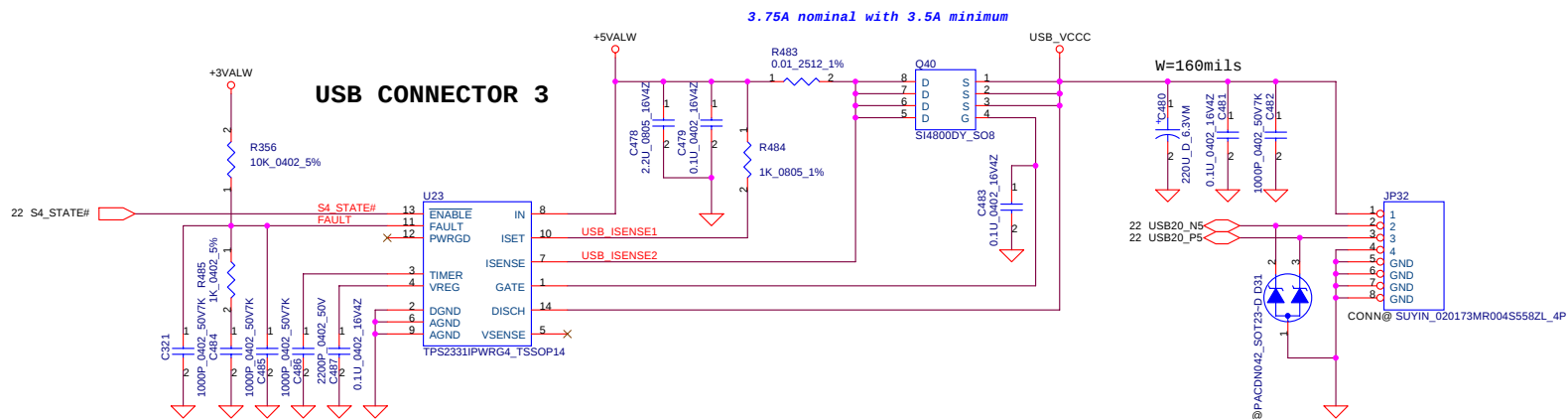
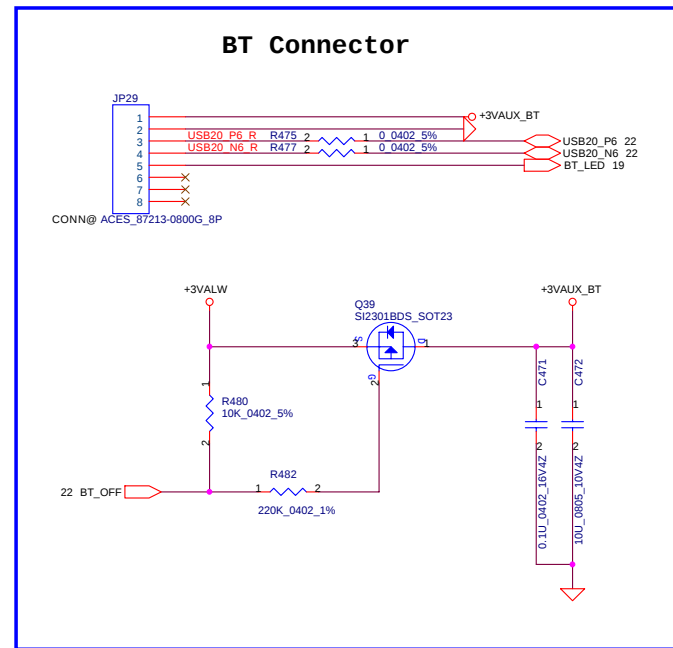
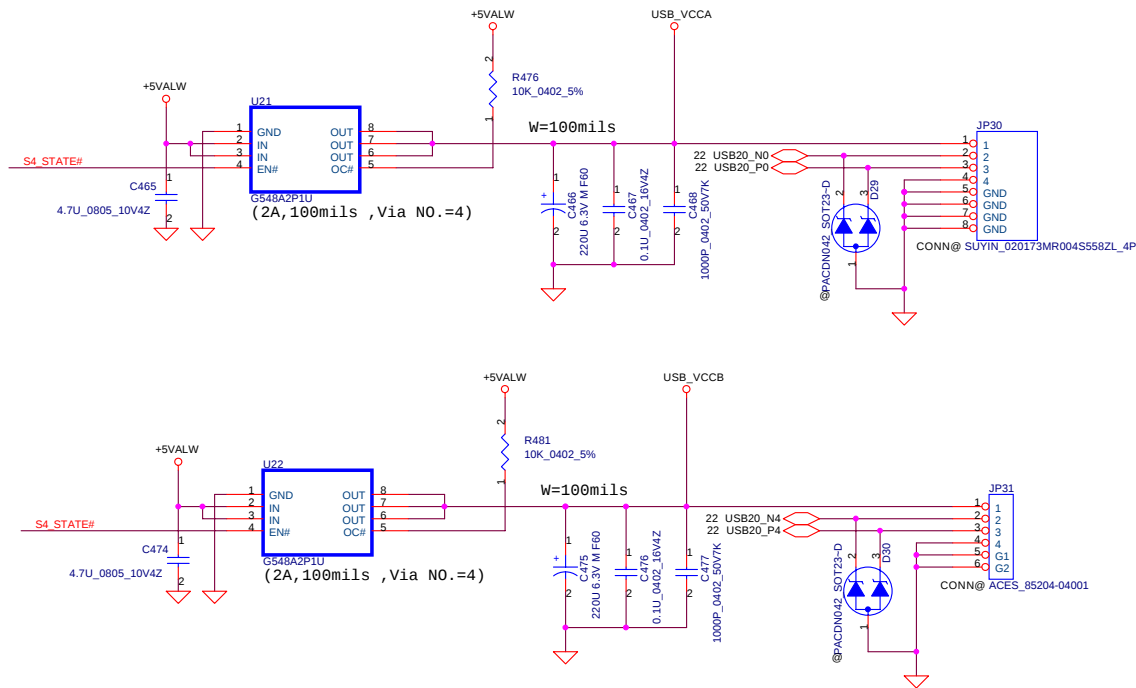
Power button



TrackPoint CONN. T/P BOARD.

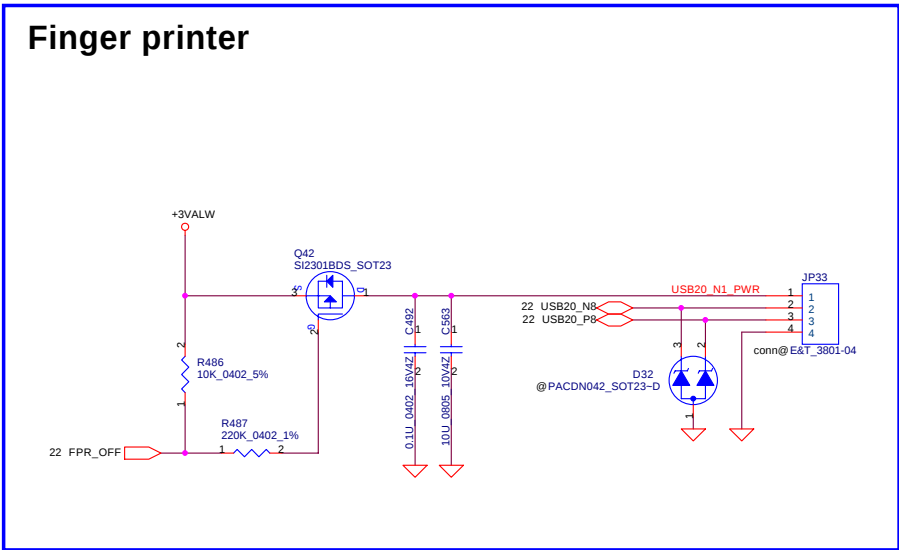
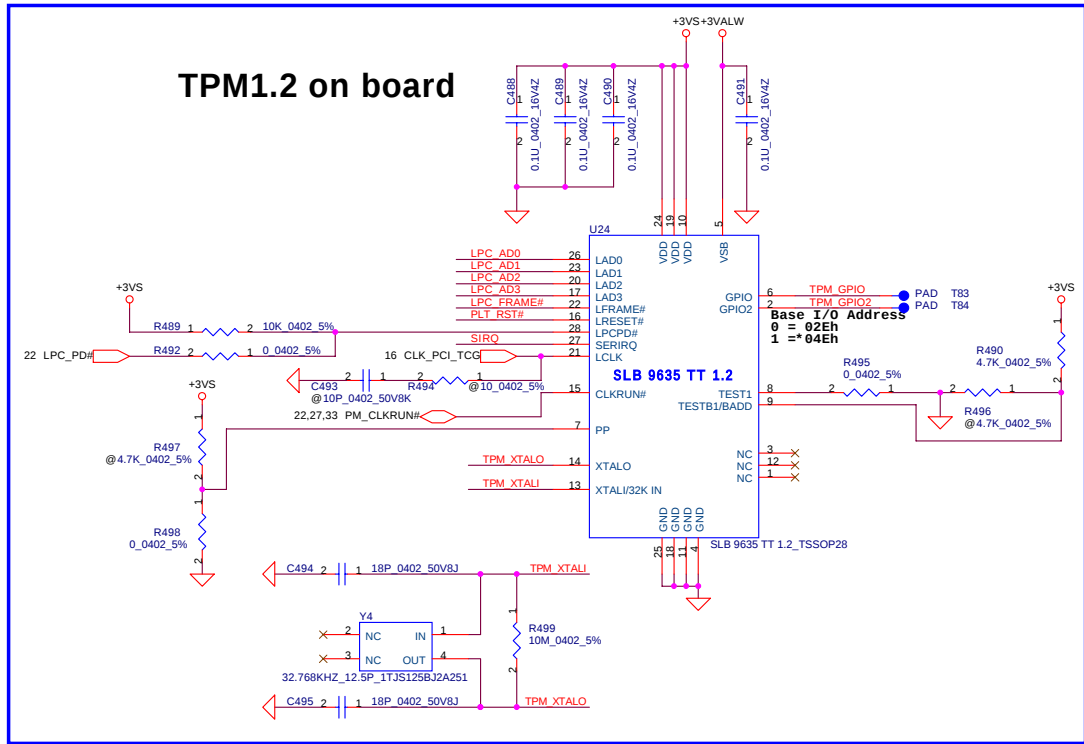


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Finger printer

[illegible]

BIOS ROM

7/20

+3VL

20mils

C496

0.1uF_0402_16V42

R501 1 2 3.3K 0402 5%

33 SPI_CS0# 33 SPI_CS0#

33 SPI_CLK 33 SPI_CLK

33 SPI_SI 33 SPI_SI

33 SPI_SO 33 SPI_SO

R503 2 1 0 0402 5%

R504 1 2 0 0402 5%

R507 1 2 0 0402 5%

R56 1 2 0 0402 5%

U25

VCC

VSS

W

HOLD

CS

CLK

SI

SO

Q

WES0_G6179-100000_8P

45@SST25LF080A_S08-200mil

U1

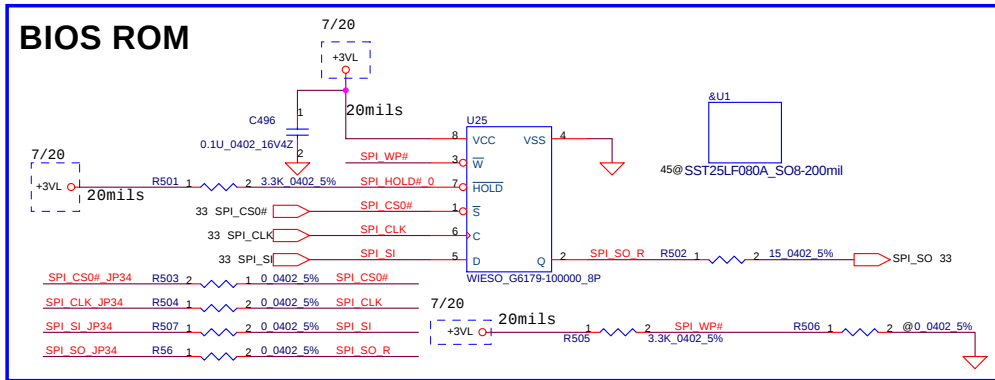
7/20

+3VL

20mils

R505 1 2 3.3K 0402 5%

R506 1 2 @0 0402 5%



LPC Debug Port

Add SIQ and connect to pin5. 10/08

8051_RECOVER#

21.6 CLK_PCL_DB

21.26,33 LPC_FRAME#

22,27,33 SIQ

8,20,26 PLT_RST#

21.26,33 LPC_AD0

21.26,33 LPC_AD1

21.26,33 LPC_AD2

21.26,33 LPC_AD3

33 8051TX

33 8051RX

33,35,39 VCC1_PWRGD

8051_RECOVER#

22.33 KBC_SPI_CS1#_R

Pin3, 23 tie to GND. 10/10

JP34

1 Ground

2 LPC_PCL_CLK

3 Ground

4 LPC_FRAME#

5 +V3S

6 LPC_RESET#

7 +VCS

8 LPC_AD0

9 LPC_AD1

10 LPC_AD2

11 LPC_AD3

12 VCC_3VA

13 PWR_LED#

14 CAPS_LED#

15 NUM_LED#

16 VCC1_PWRGD

17 SPI_CLK

18 SPI_CS#

19 SPI_SI

20 SPI_SO

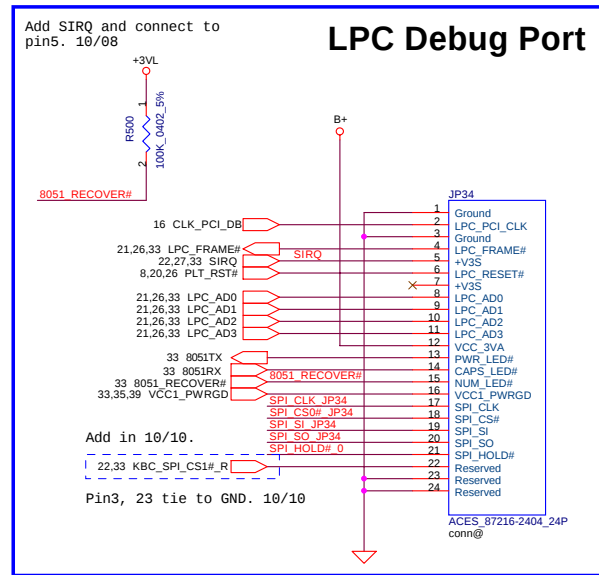
21 SPI_HOLD#

22 Reserved

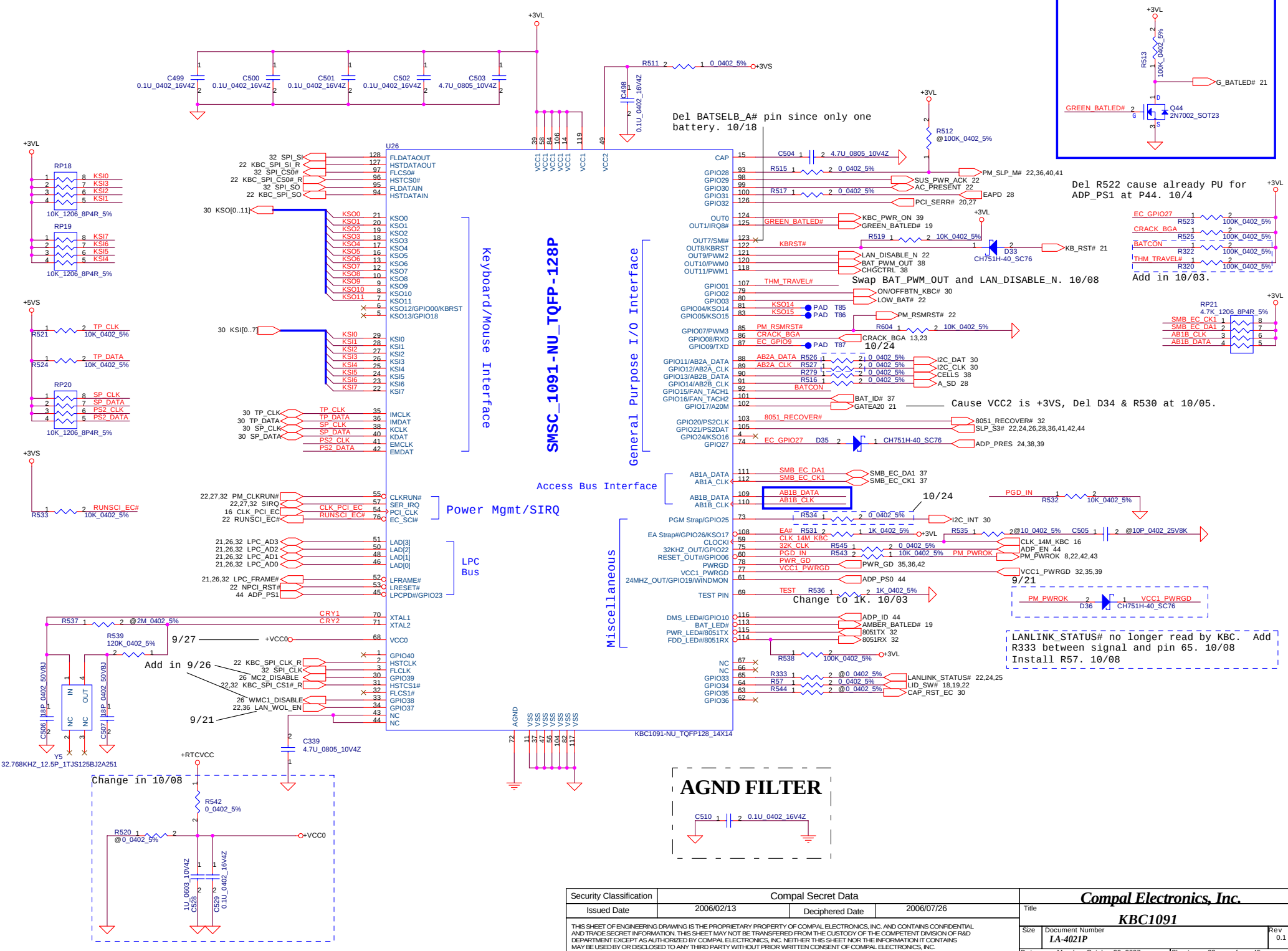
23 Reserved

24 Reserved

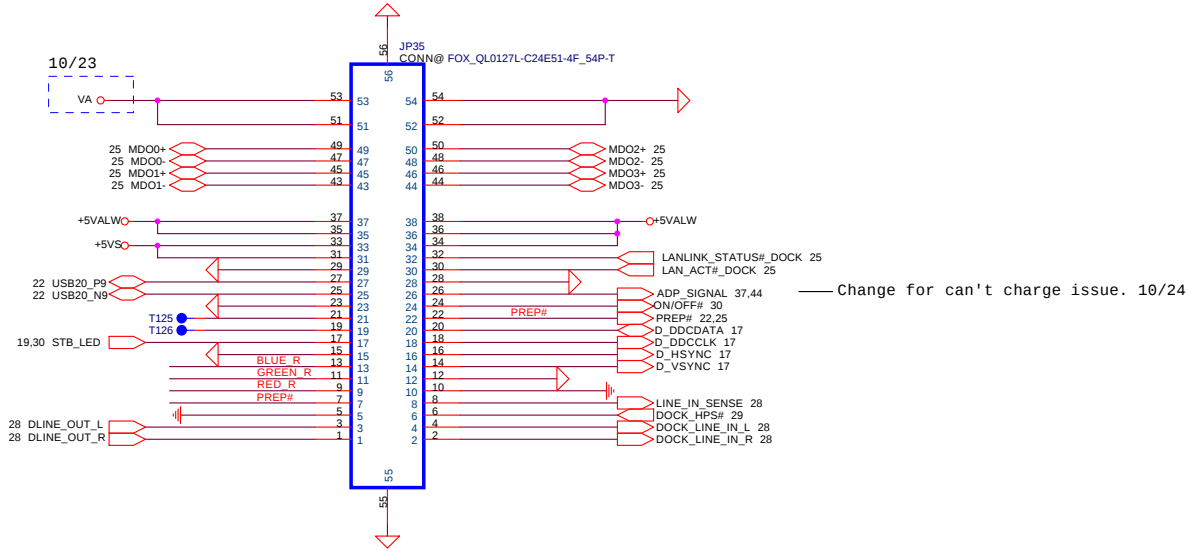
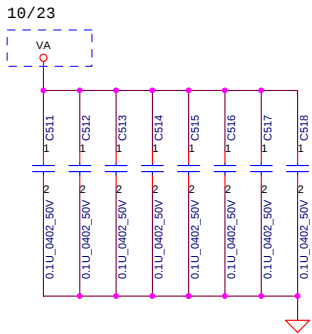
ACES_87216-2404_24P conn@



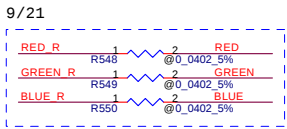
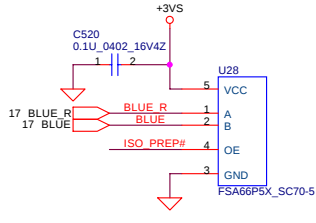
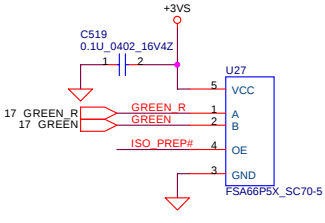
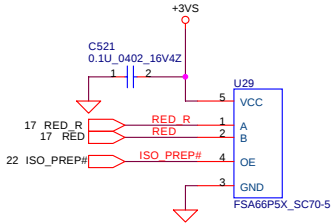
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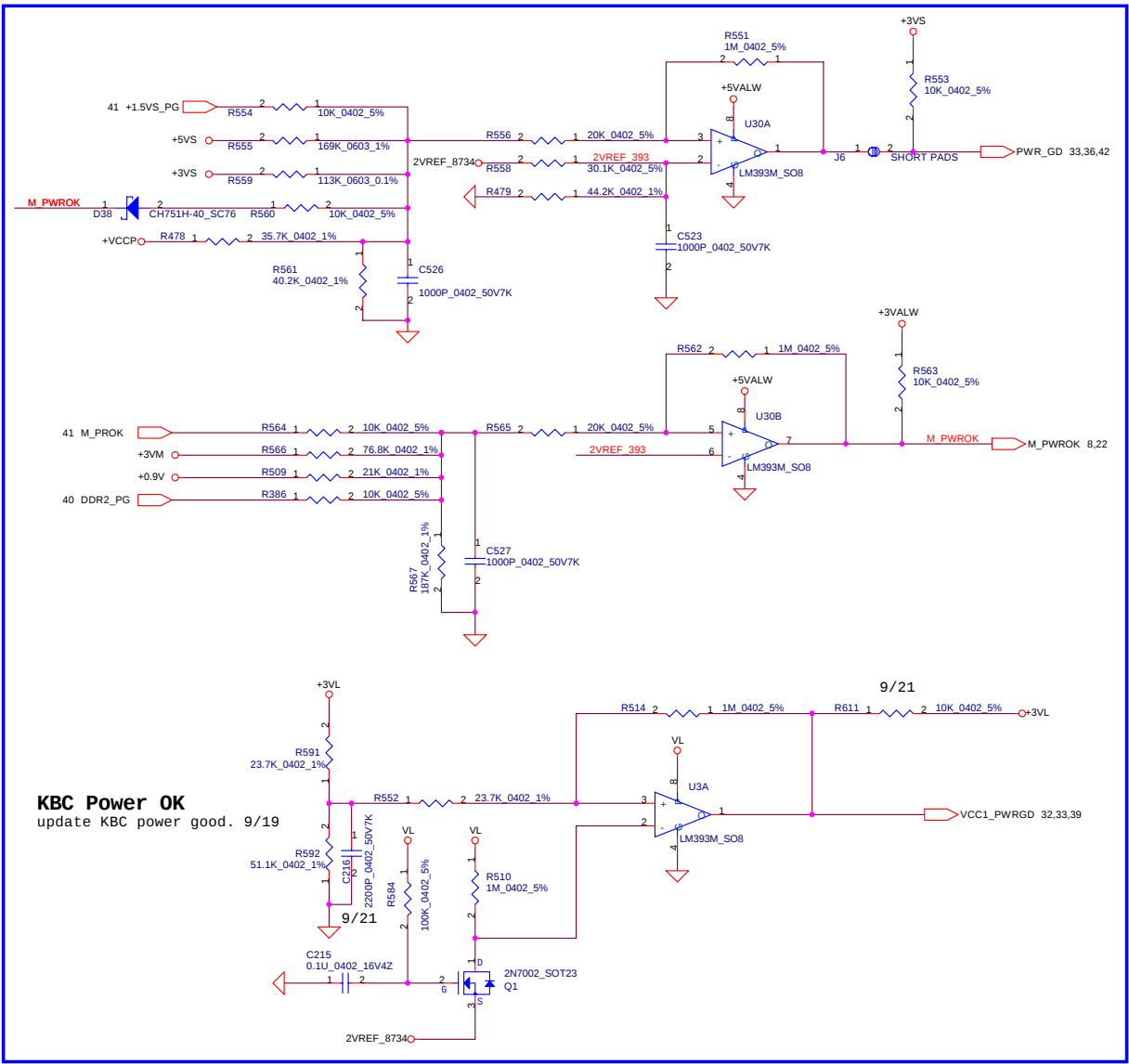
DOCKING CONNECT



Del R610, Q43. 10/24



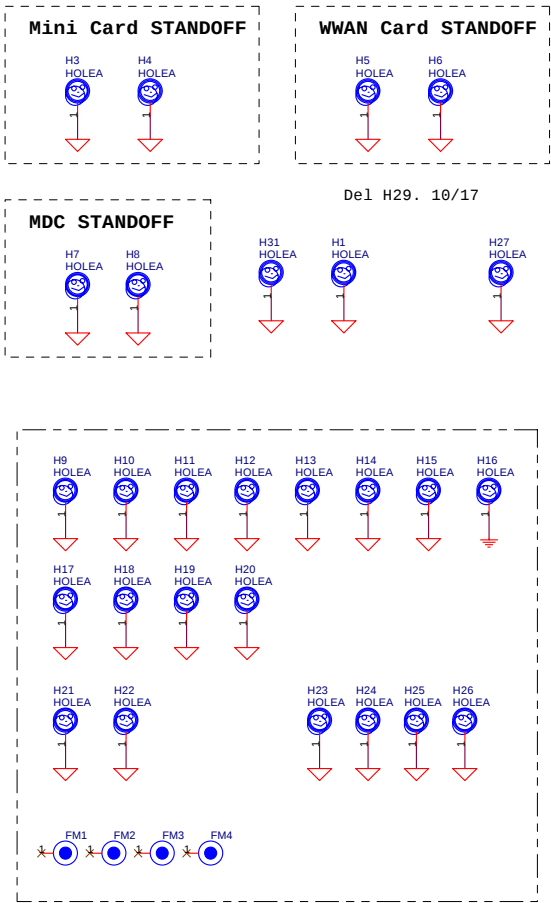
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KBC Power OK

update KBC power good. 9/19

9/21

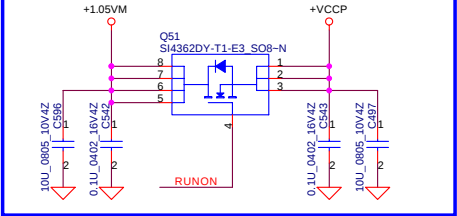


Del LAN reset schematic. 9/26

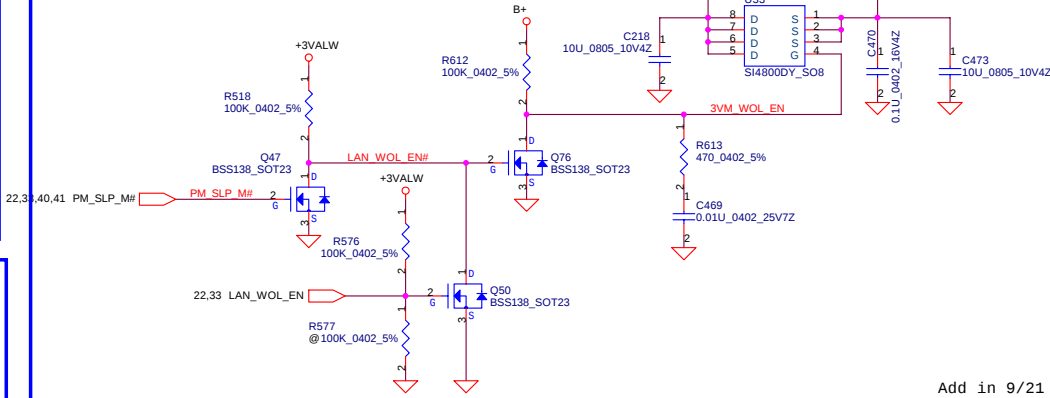
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				Size	Document Number	Rev
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Modify at 7/31 after discuss with power team.

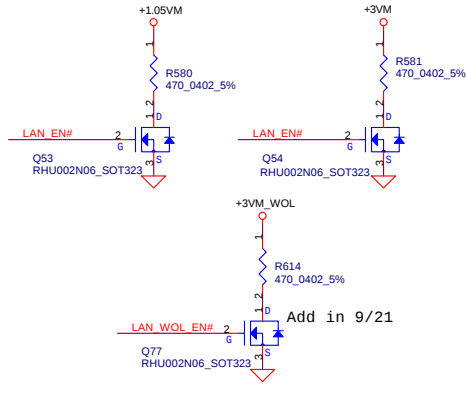
+1.05VM to +VCCP Transfer



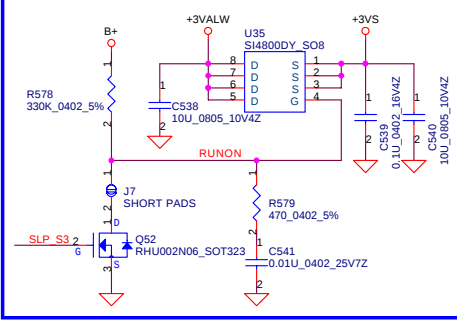
+3VALW to +3VM_WOL Transfer



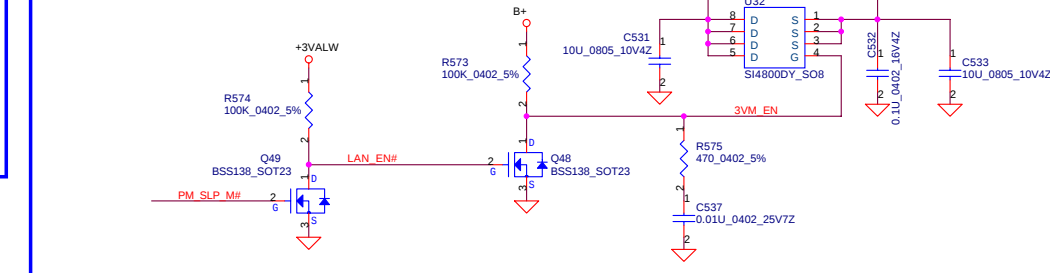
Discharge circuit-2 for V-M



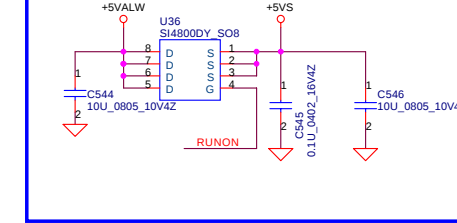
+3VALW to +3VS Transfer



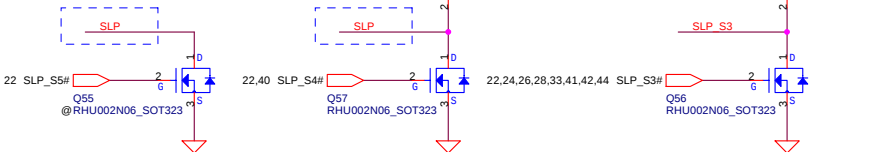
+3VALW to +3VM Transfer



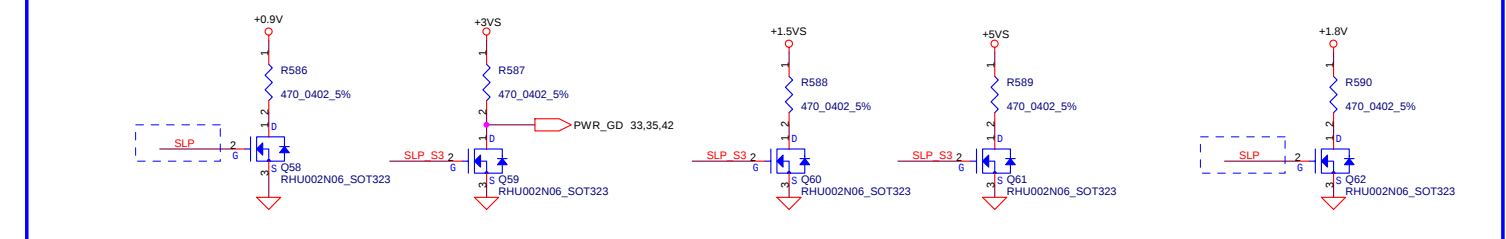
+5VALW to +5VS Transfer



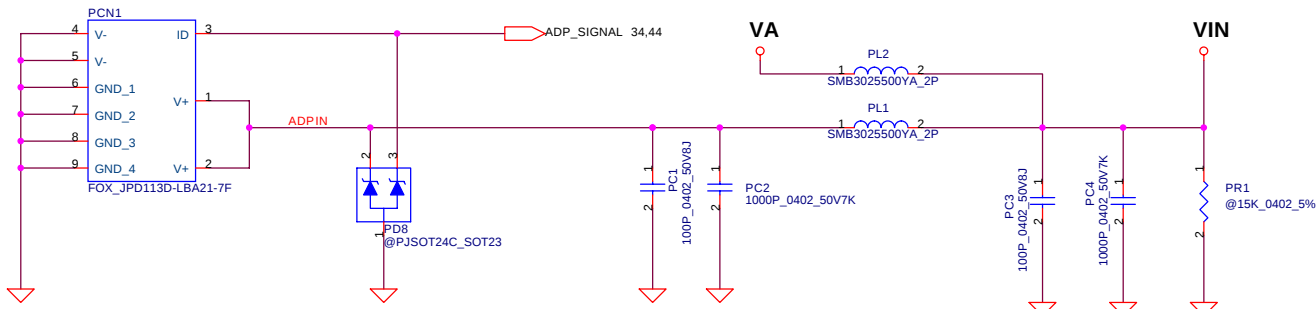
Design Change at 9/14.



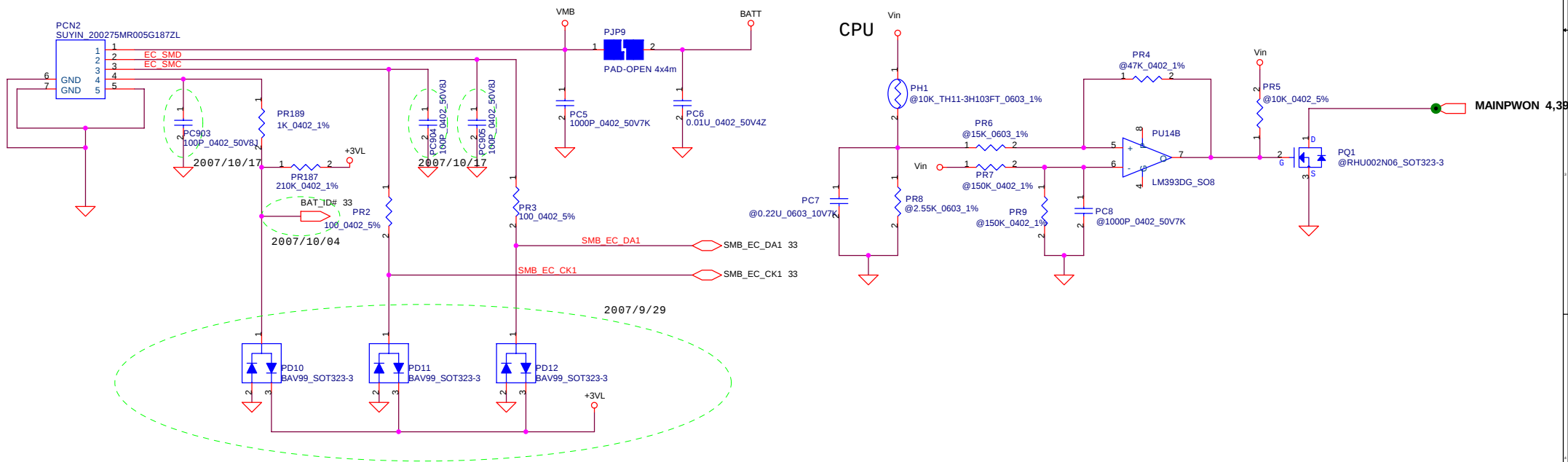
Discharge circuit-1



SYS. STATE	PM_SLP_M#	LAN_WOL_EN	+3VM_WOL	+3VM
M-off / No WOL	0	0	0V	0V
M-off / WOL	0	1	3.3V	0V
M1 (ME on)	1	0	3.3V	3.3V
M1 (ME on)	1	1	3.3V	3.3V

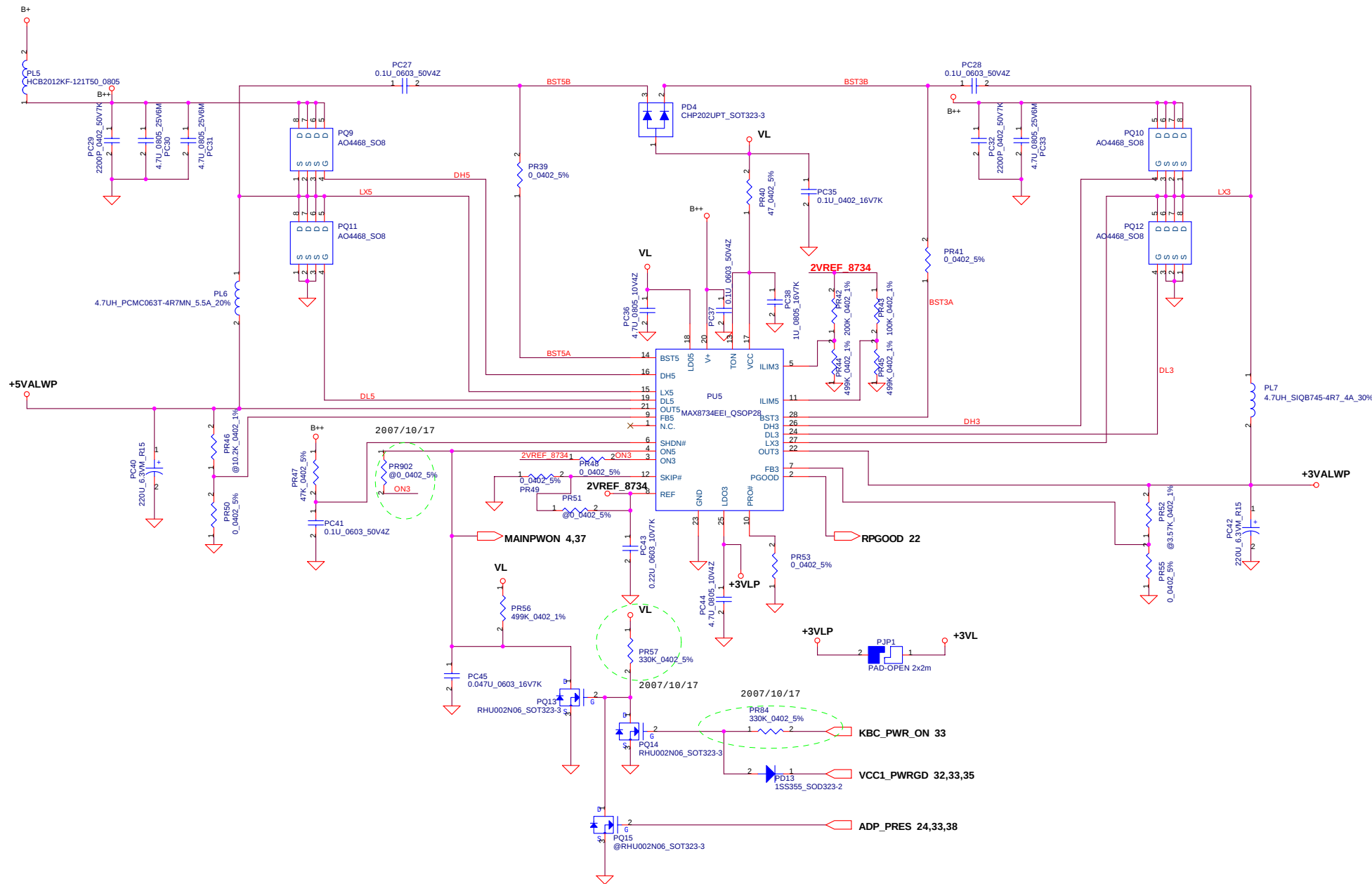


PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 47 +-3 degree C

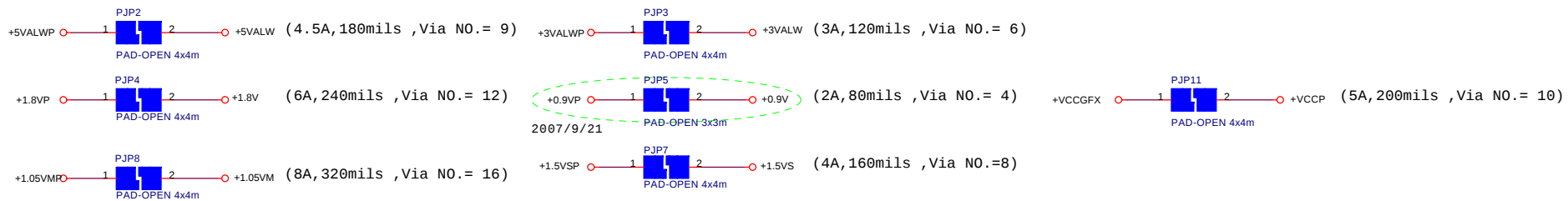
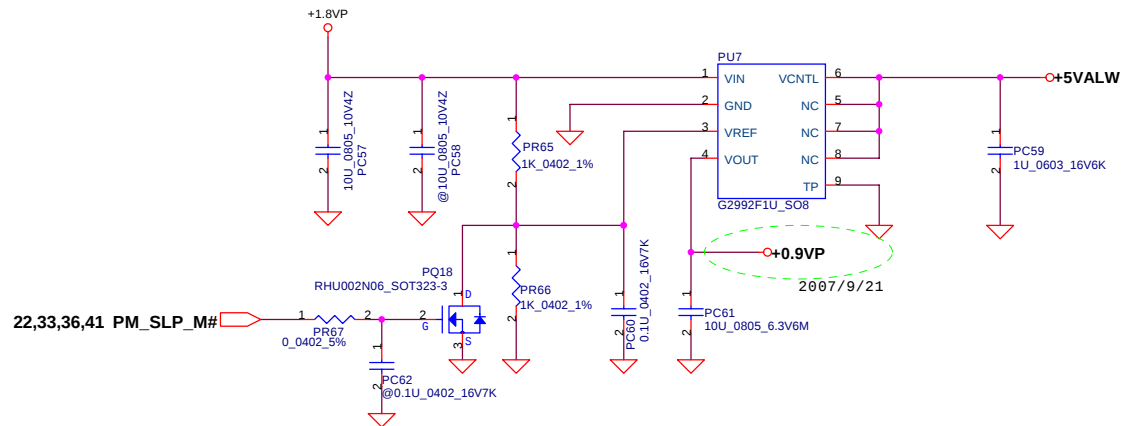
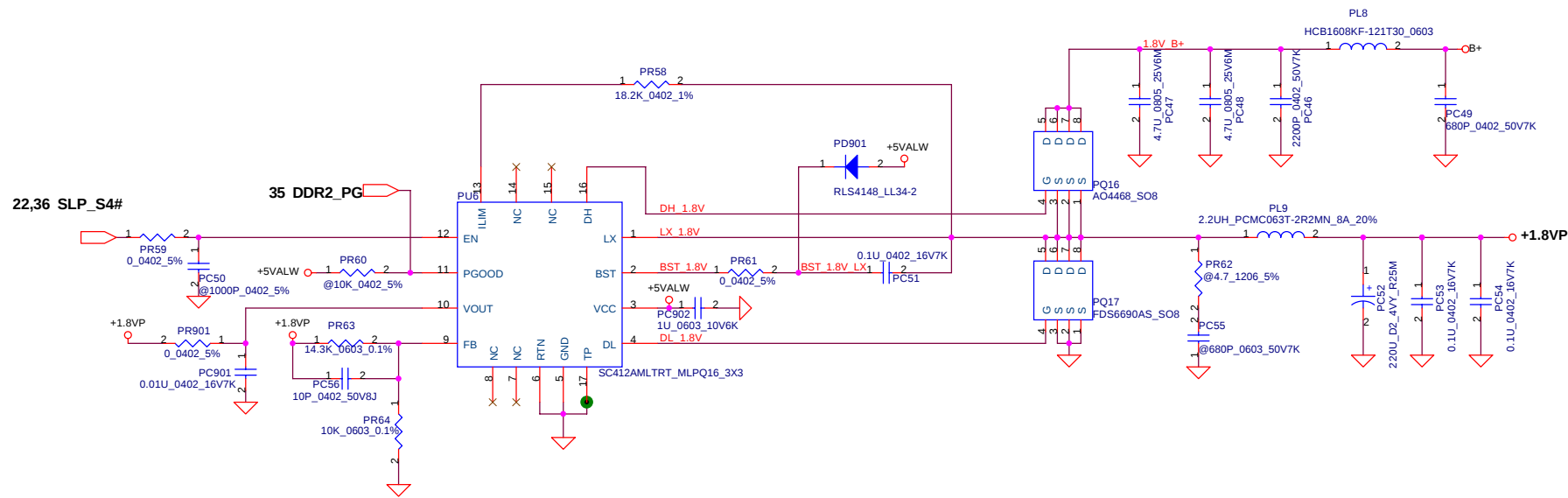


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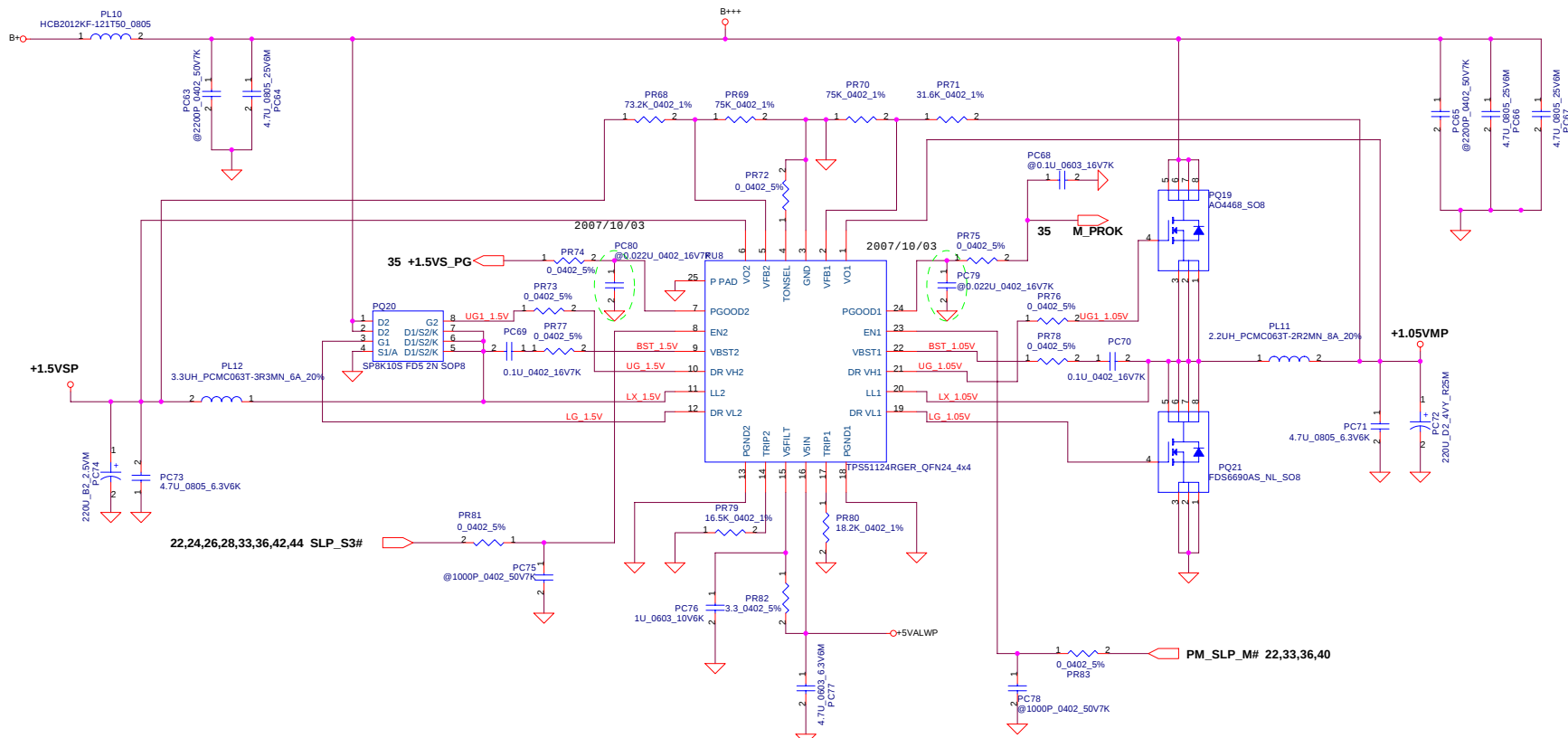
+3.3V/+5V



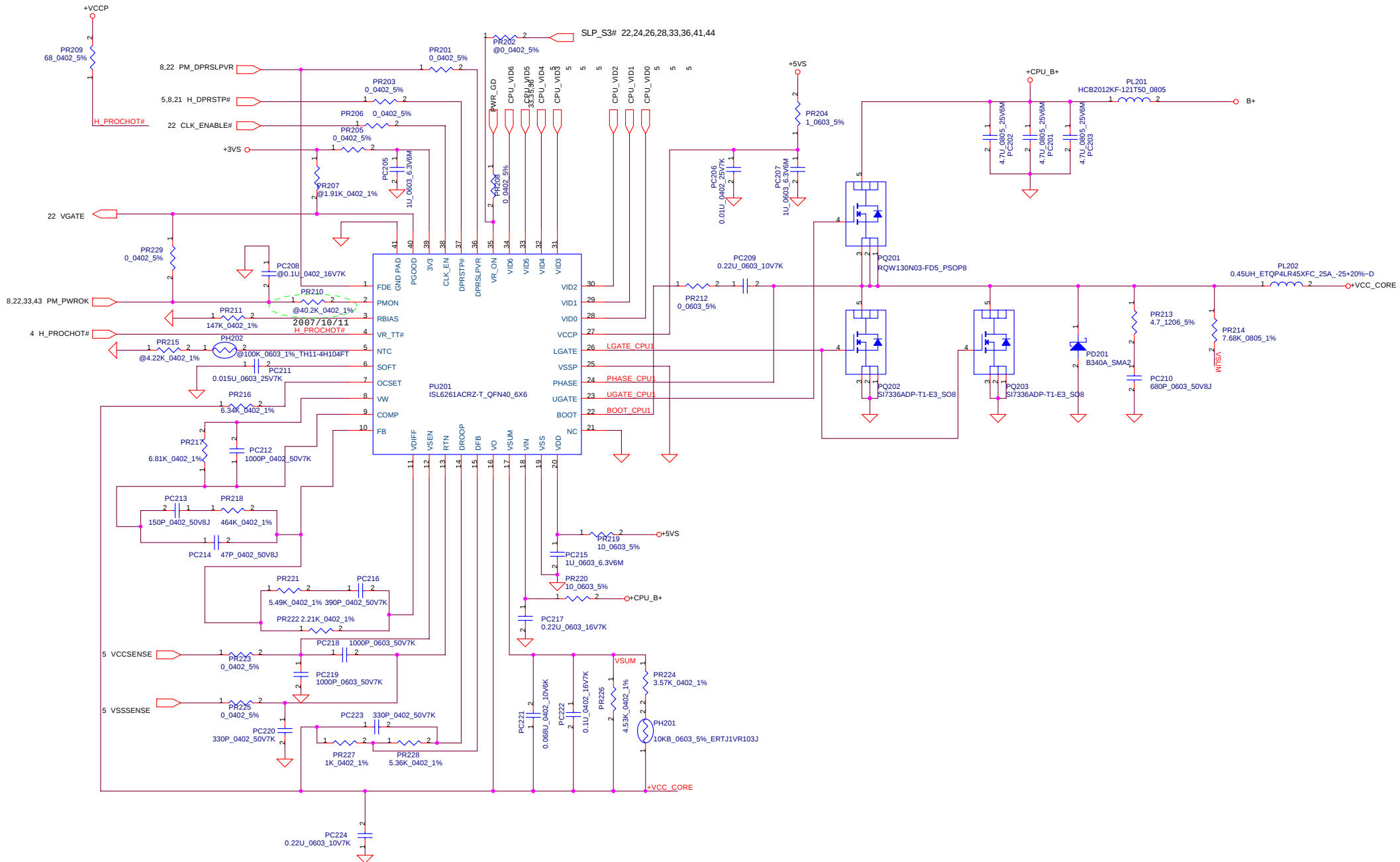
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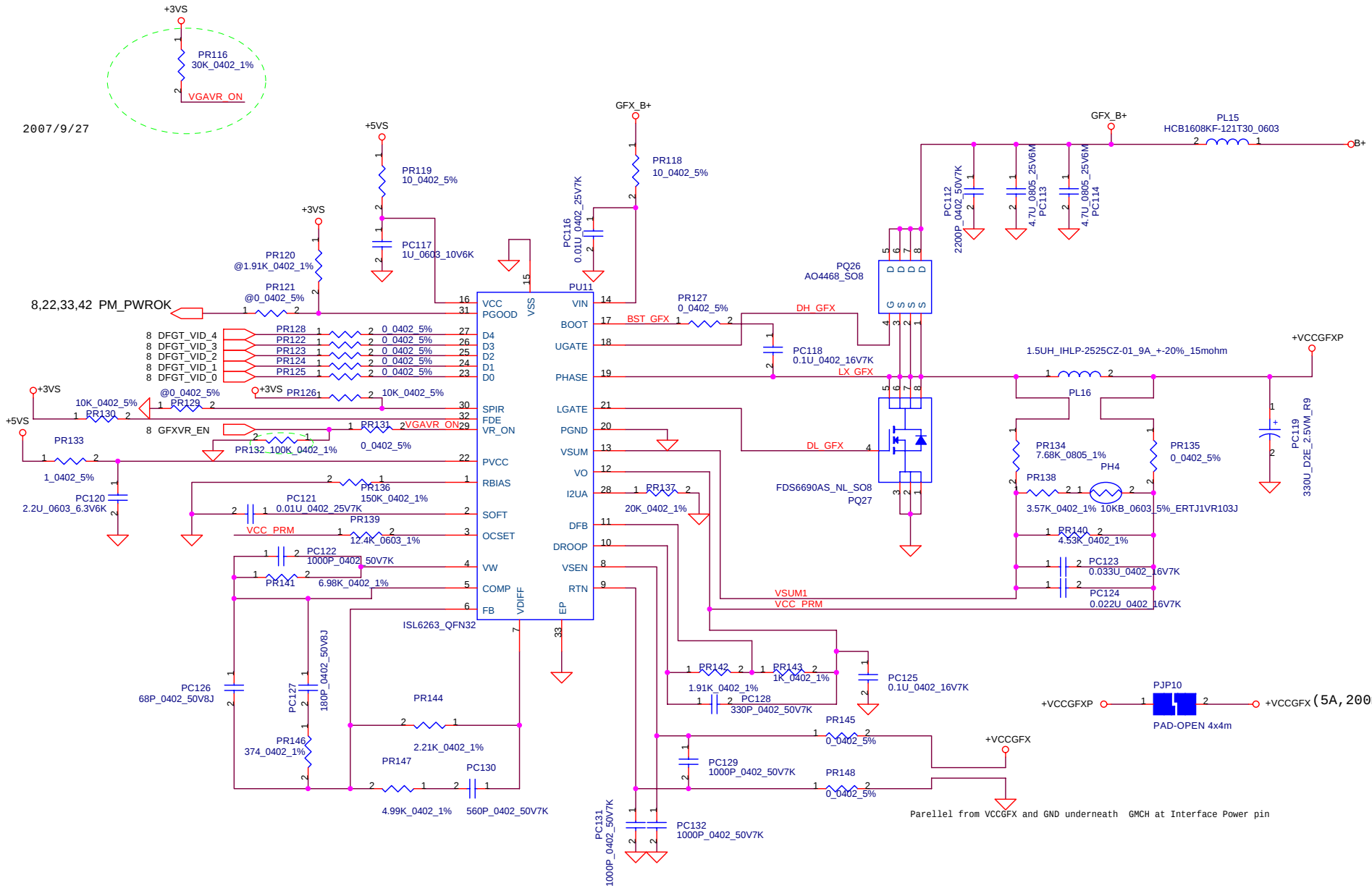


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Size	Document Number	Rev			0.2
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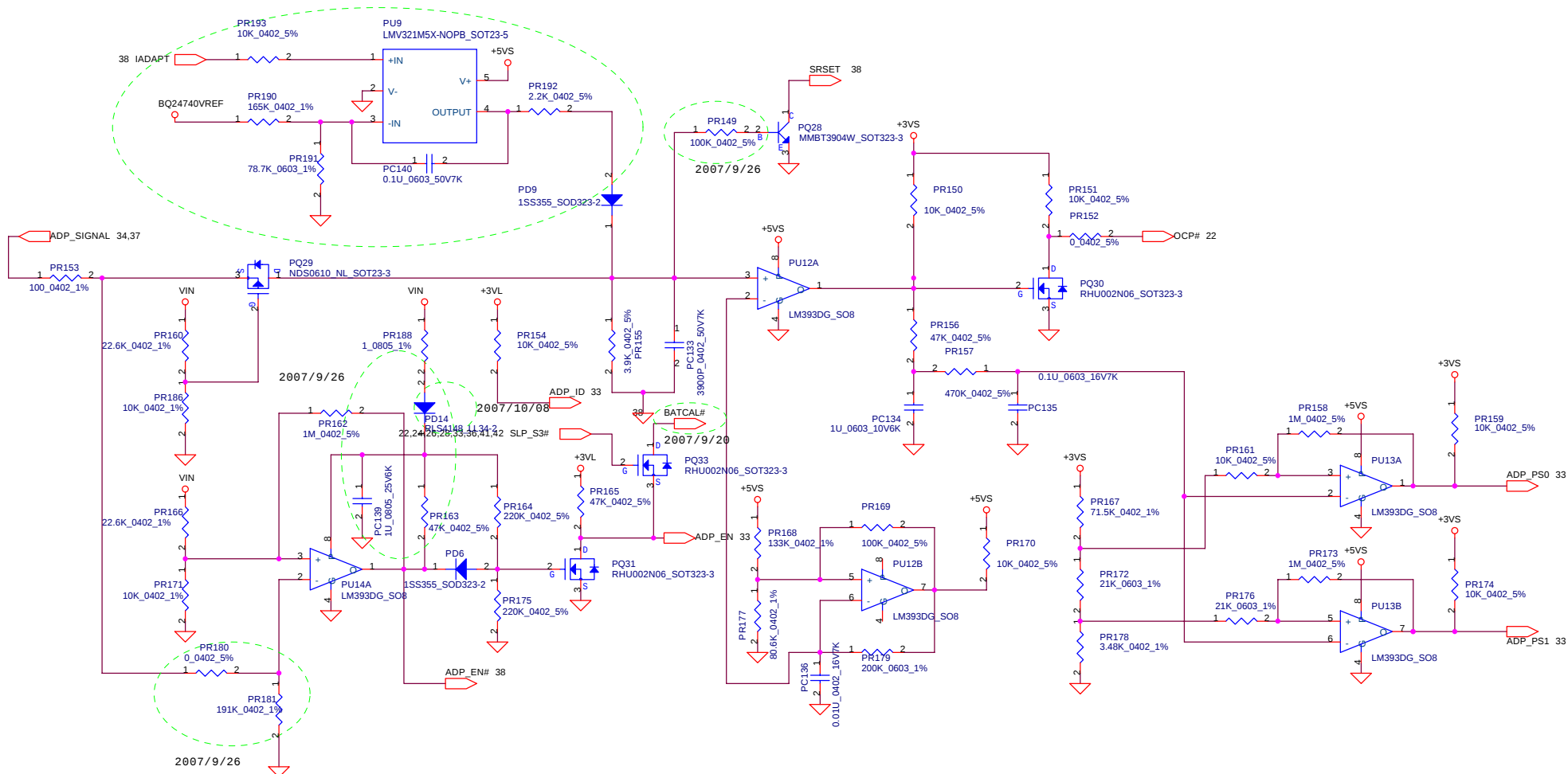
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